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RADC-TR-78-267
Final Technical Report
January 1979

PRELIDDING BURN—IN EVALUATION

Raytheon Company

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-78-267	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): PRELIDDING BURN-IN EVALUATION	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report 25 Oct 76 - 31 Mar 78
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): James R. DiNitto, Klaus B. Lasch	8. CONTRACT OR GRANT NUMBER(s): F30602-77-C-0004
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Raytheon Company, Hartwell Road, Bedford MA 01730	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 23380103
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRM), Griffiss AFB NY 13441	12. REPORT DATE: January 1979
	13. NUMBER OF PAGES: 99
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: John Farrell (RBRM)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Hybrid Circuits
Screening
Prelidding Burn-In
Parametric Shift Analysis

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Screening of hybrid circuits is designed to identify and eliminate early electrical failures. Rework of these failures is complicated by the fact that the hybrids are sealed. This evaluation was designed to determine whether or not it is feasible to perform part of the burn-in portion of the screening sequence prior to package sealing. A hybrid circuit was designed to incorporate a wide range of components and materials and to permit access to points

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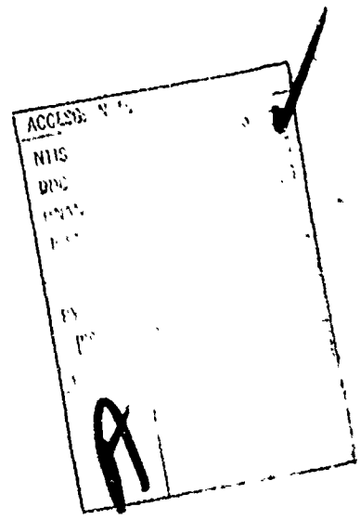
internal to the circuit for parametric shift detection. A test plan was devised to assess the efficiency of performing prelid burn-in under various conditions and to verify that no long term deleterious effects were introduced. Results of this evaluation have shown that prelidding burn-in is effective and is non-destructive. It should be performed in a dry nitrogen, Class 10,000 maximum, environment at 125°C for 48 hours. Sealed lid burn-in should be performed after prelidding burn-in at 125°C. Total minimum burn-in time of 160 hours at 125°C can be divided between prelidding and sealed lid burn-in provided that the total burn-in time equals or exceeds the specified 160 hour burn-in time equals or exceeds 96 hours. A MIL-STD-883 method should be prepared to define the proper conduct of prelidding burn-in.



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EVALUATION

The purpose of this effort, which supports RADC TPO-R5B, "Solid State Device Reliability," was to evaluate the factors related to prelidding burn-in that could affect the reliability of hybrid microcircuits.

The program results, detailed in the report, are considered highly successful in defining test limits, conditions and usage guidelines, including precautions to be exercised for the prelidding burn-in of hybrid microcircuits. The test data indicates that properly controlled prelidding burn-in is non-destructive and effective. However, to be cost effective, it should be selectively applied using circuit complexity, known inherent problems and past history, if available, as selection criteria. The results also show that significant electrical parameter changes, primarily in MOS devices, occurred whether lidded or unlidded burn-in was performed. The significant number of failures due to handling problems points out the importance of imposing special provisions for device covering and transfer.

RADC, the Preparing Activity for MIL-STD-883, "Test Methods and Procedures for Microelectronics," is responsible for studying and updating microcircuit quality assurance procedures to provide reliable, accurate and cost effective test methods. Results of this effort will be used to prepare a prelidding burn-in test method for MIL-STD-883.

JOHN P. FARRELL
Project Engineer

I. INTRODUCTION

Burn-in testing is performed on hybrid devices to screen or eliminate marginal devices and those with manufacturing defects that can lead to time and stress dependent failures. By stressing hybrid devices at or above maximum rated operating conditions these defective devices can be identified. If burn-in testing is not performed, these defective devices would be expected to fail early under these conditions.

Burn-in testing is normally performed after hybrid devices have been completely assembled and sealed. Sealed devices that fail burn-in testing, and are candidates for rework, must be exposed to a delidding operation which may cause damage to the device package or to included components. Devices that are fabricated to MIL-M-38510D requirements, however, cannot be delidded for the purposes of rework so that early failures have to be scrapped. It would be desirable to perform part of the burn-in testing prior to package lidding so that rework, if necessary, can be readily accomplished without possible package or component damage caused by delidding. The primary cause of failure of hybrid devices are the attached components which are not available preburned-in. Identification and replacement of these faulty components prior to lidding potentially can have a favorable effect on the yield, cost and availability of hybrid microelectronics.

The purpose of this evaluation was to provide information concerning the effectiveness of prelidding burn-in. It sought to provide specific details concerning allowable temperatures, time durations and ambient environments. It sought further to identify possible prelidding burn-in related long-term effects on device electrical characteristics.

Acknowledgement - This report was written under Contract Number F30602-77-C-0004 with the Air Force System Command's Rome Air Development Center, Griffiss Air Force Base, New York.

II. HYBRID CIRCUIT TEST VEHICLE

2.1 Circuit Design

To study the questions posed by the performance of prelidding burn-in, a functional hybrid circuit test vehicle was designed. The criteria used for the circuit design were many. Specifically, the test vehicle had to:

1) be representative of a typical hybrid circuit in complexity and and function.
2) incorporate both thick and thin film technologies.
3) incorporate bi-polar and MOS integrated circuits (both digital and analog devices), PNP, NPN and MOS transistors (both small signal and power), diodes, capacitors and resistor chips.
4) incorporate both gold and aluminum wire interconnects.
5) incorporate both eutectic and epoxy mounted devices.
6) be simple to test and failure diagnose.
7) be simple to burn-in.
8) be relatively simple in design to maximize yield.
9) be housed in a package which could be hermetically sealed.

With the above criteria in mind, the circuit concept shown in Figure 1 was developed. With only DC power applied to the device, the following actions would take place within the device itself. An oscillator would feed an amplifier, which in turn would drive two voltage comparators. The signal out of one comparator would drive four TTL flip flops connected in series. The output from the last flip flop would connect to an external load network consisting of thick film resistors and switching diodes. The signal out of the other voltage comparator would feed a series of four CMOS gates. The output from the last gate would connect to an external load network consisting of resistors and Schottky diodes. The circuit would be serviced by a voltage regulator, which would develop +5 volts DC from a +12 volt DC input. In essence, this circuit was designed to exercise itself.

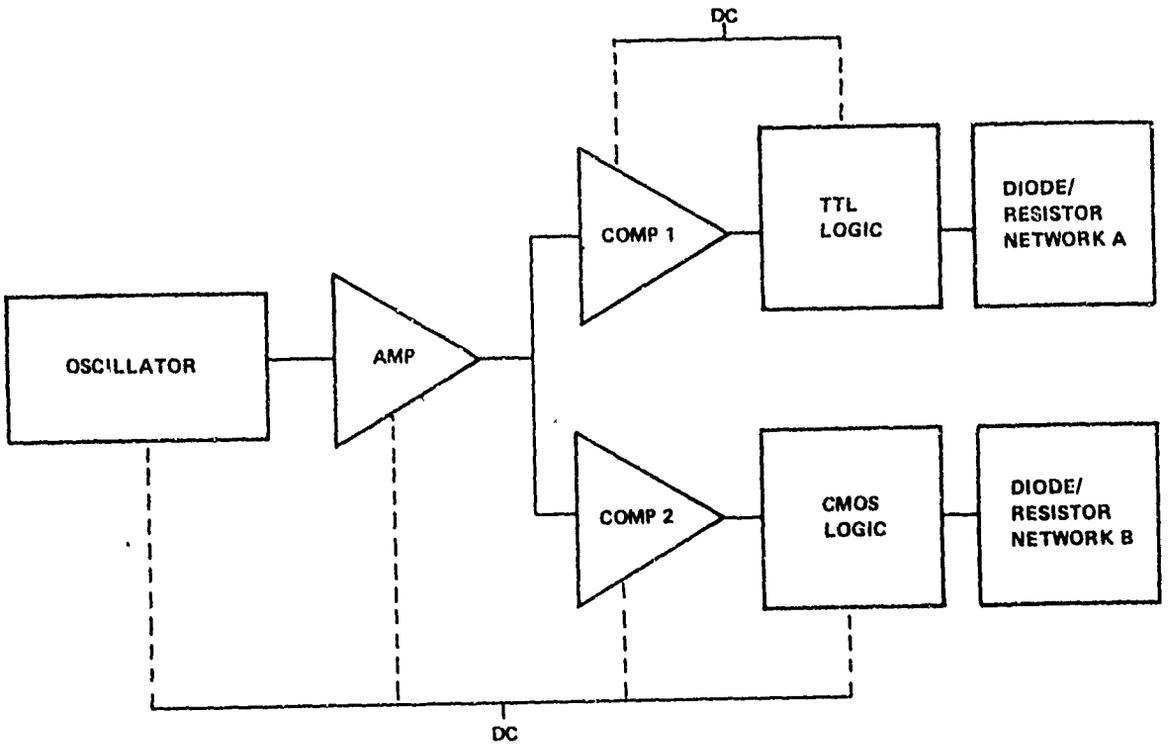


Figure 1. Test Vehicle Circuit Concept

Using discrete components, a breadboard model was built to evaluate the concept. After much testing, the circuit was finalized as shown in Figure 2. The test points that were to be used later in the electrical testing of the completed devices were planned at this time and were located as indicated in Figure 2.

2.2 Device Fabrication

The test vehicle design called for incorporation of a wide range of chip components as shown in Table 1. Photomacrographs of each of the active devices are included in Appendix A. The test vehicles were fabricated using standard thick film technology. The parts and materials incorporated are shown in Table 2. The baseline assembly process used conductive, silver-filled epoxy chip attach and ultrasonic gold-wire bonding.

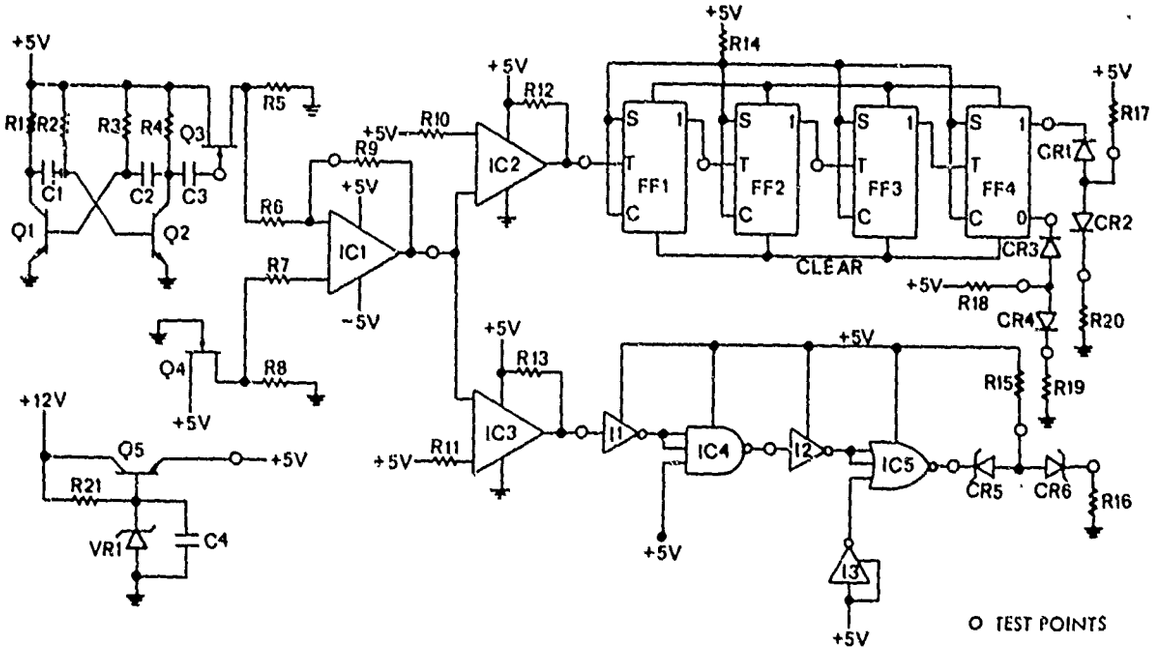


Figure 2. Finalized Test Vehicle Circuit Diagram

TABLE 1

CHIP COMPONENTS INCORPORATED

Chip Description	Chip Type	Number Used
Linear IC, bi-polar	LM741	1
Linear IC, bi-polar	LM139	1
Digital IC, CMOS	CD4007	3
Digital IC, LSTTL	54LS112	2
Transistor, bi-polar	2N2222	2
Transistor, bi-polar	2N4237	1
Transistor, FET	2N3957	1
Diode, diffused	1N3600	4
Diode, Schottky	HP5082-0087	2
Diode, Zener	1N5232	1
Resistor, thin film	10 KΩ	3*
Resistor, thin film	100 KΩ	3
Capacitor, ceramic	0.01 μF	2
Capacitor, ceramic	0.001 μF	2

*One thin film resistor network containing three resistors

TABLE 2

PARTS AND MATERIAL INCORPORATED

Part or Material	Description
Substrate	96% Alumina, 1" x 1"
Conductor ink	Dupont 9791
Resistor ink	Dupont 1431, 1KΩ
Resistor ink	Dupont 1451, 100KΩ
Overglaze	Dupont 9137
Package	Isotronics plug-in type with lid, 1.25" x 1.25"
Tab	Molybdenum
Preform	Gold Germanium
Conductive epoxy	Ablestick 36-2
Non-conductive epoxy	Ablefilm 500
Wire	Aluminum, 1 mil diameter
Wire	Gold, 1 mil diameter

In order to broaden the technologies incorporated, the 2N4237 power transistor in the voltage supply was gold silicon eutectic premounted to a gold plated molybdenum tab. This was in turn mounted on the substrate using a gold germanium preform. One set of diodes, the 1N3600s in the low power Schottky IC network, was gold silicon eutectic mounted directly to the substrate. Ultrasonic aluminum wire bonding was used to bond the two flip flop IC chips. The completed substrate was epoxy attached to the package, which was a 30 pin, welded, plug-in type. This package was selected because Raytheon had favorable past experience with it and because all necessary fixtures were on hand. All of the processing considerations discussed above were controlled by a process flow chart, in which the unique processing sequence developed for the hybrid circuit test vehicle was controlled. Each operation in the sequence was itself controlled by an operation standard.

After component attachment, the substrates were then packaged and wire bonded. The devices, one of which is shown in Figure 3, were then electrically tested to verify that they were functional. A test box, which, used a zero insertion force test socket, was constructed to facilitate this functional testing which revealed such reworkable defects as missing wire bonds and damaged chip components.

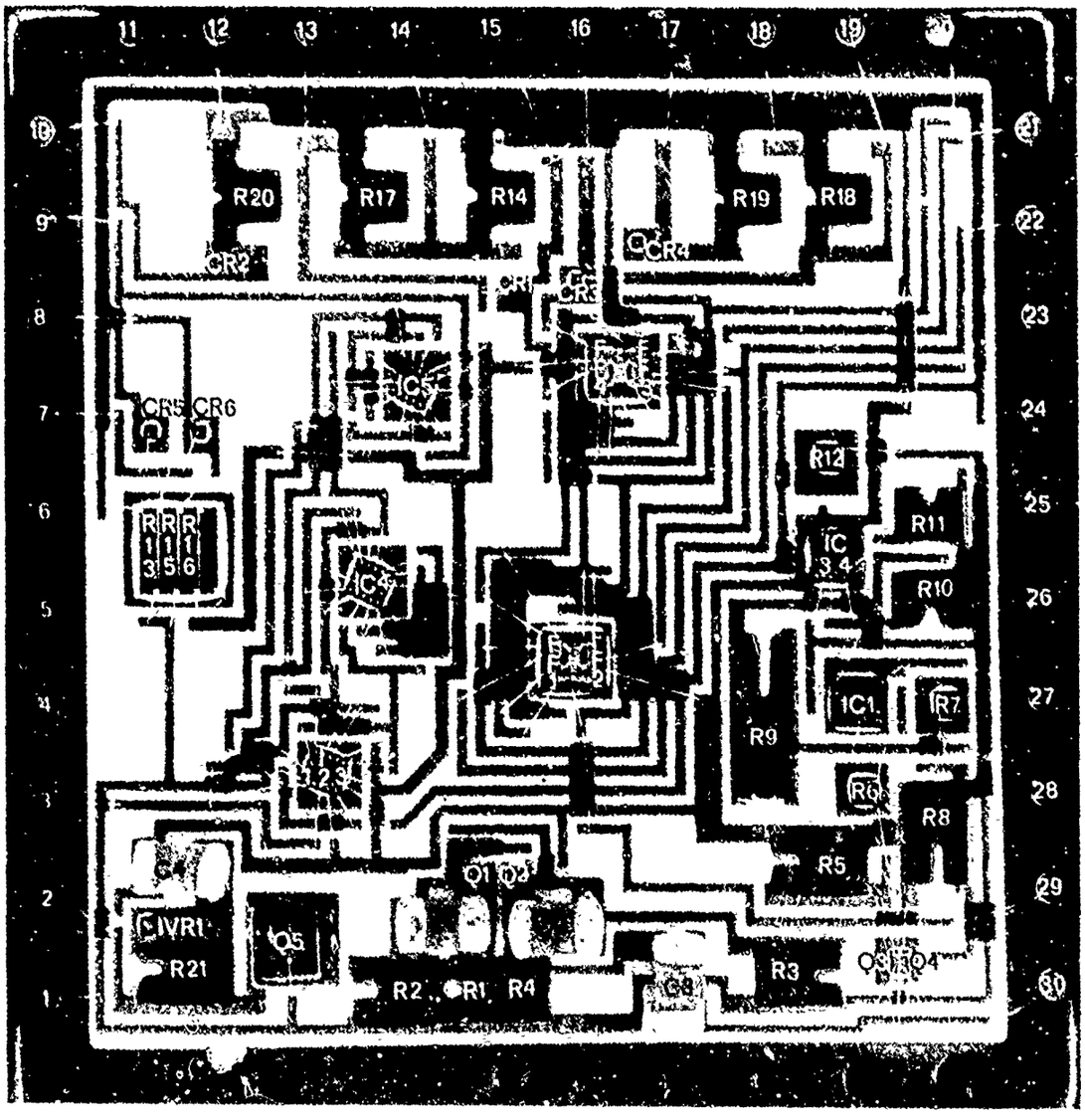


Figure 3. Completed Hybrid Circuit

At the completion of prelidding burn-in testing, which is discussed in detail in the next section, the package covers were seam welded onto the packages. The seam welder itself was placed in the dry box shown in Figure 4, which was equipped with ovens that opened directly into it. The dry box and the ovens were filled with dry nitrogen. The moisture content of the dry nitrogen was constantly monitored and, typically, was ten parts per million or less. Stabilization baking and sealing of the test vehicles was performed in the same carefully controlled environment. A typical sealed hybrid circuit test vehicle is shown in Figure 5.

Ultimately, a total of 157 devices were assembled and serially numbered. Of this number, 141 were used in the burn-in testing, one became a master test control device, four were used for bond strength testing and two were used for gas analysis. The remainder were not utilized and were never sealed.

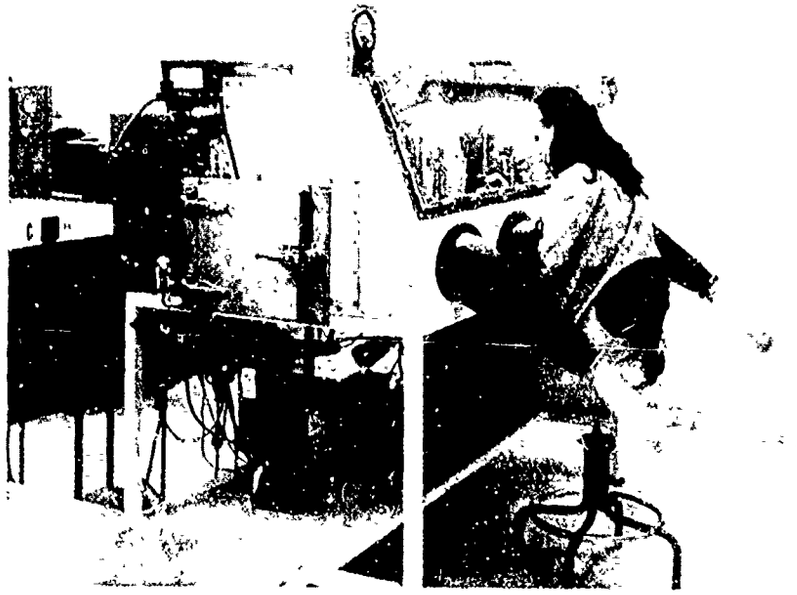


Figure 4. Dry Box

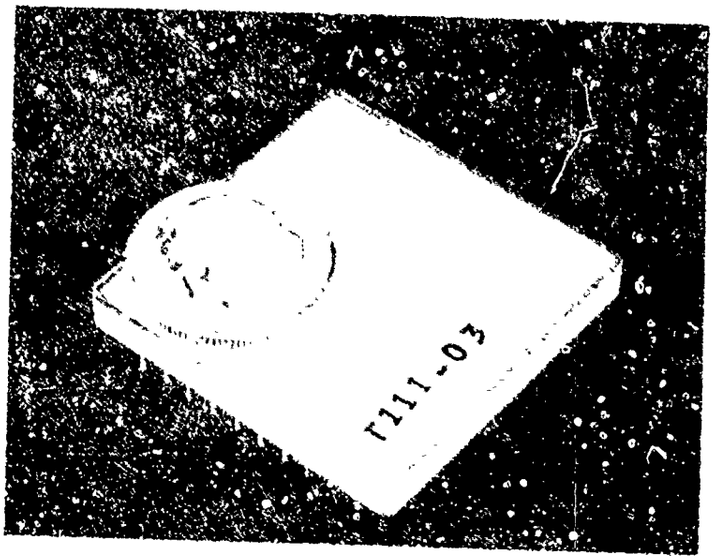


Figure 5. Sealed Hybrid Circuit Test Vehicle

III. BURN-IN TESTING

3.1 Specific Considerations

After assembly operations were completed, and prior to sealing of the hybrid circuit test vehicles, prelidding burn-in testing was performed. This testing, as well as the sealed lid burn-in testing and the life and accelerated testing, is discussed chronologically in detail below. The burn-in test circuit used for all this testing is shown in Figure 6. Burn-in test racks were constructed that utilized high temperature resistant sockets. Figure 7 shows a typical burn-in rack.

For the prelidding burn-in portion of the evaluation, a brand-new burn-in oven was utilized to assure optimum cleanliness conditions. This oven was specially modified so that a dry nitrogen environment could be created for use during prelidding burn-in testing. Prior to the start of prelidding burn-in, the oven was run at temperature with empty burn-in racks in place. Dry nitrogen (less than ten parts per million water vapor) was allowed to flow through the oven. Particle counts were taken of the nitrogen flowing out of the oven. These revealed that Class 10,000 nominal conditions existed. It was decided to leave the oven on with the nitrogen purge for an extended time in the hope that the particle generation would

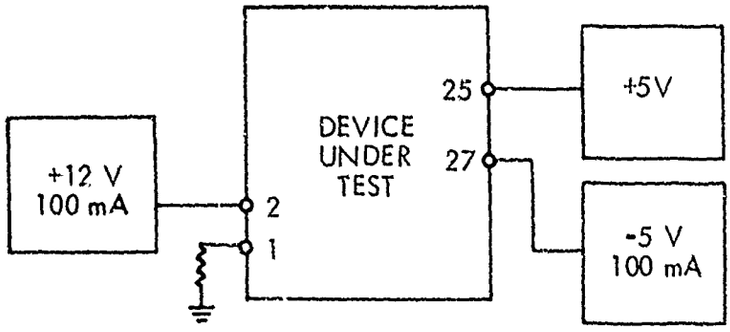


Figure 6. Burn-in Test Circuit

become exhausted; however over two weeks of this, no significant improvement was noted. It was concluded that, evidently, there are particulating materials used in the manufacture of standard ovens which preclude attainment of Class 100 environment when operated in a normal mode. It was found, however, that Class 100 conditions could be attained with the oven circulating fan shut off. To preclude compromise of the evaluation, one group of test devices was split in two. One half was prelid burned-in with the fan on (or in a Class 10, 000 nominal environment) and the other half was prelid burned-in with the fan off (or in a Class 100 nominal environment). For the sealed lid burn-in testing and the life and accelerated testing, a standard, unmofidied burn-in oven was utilized.

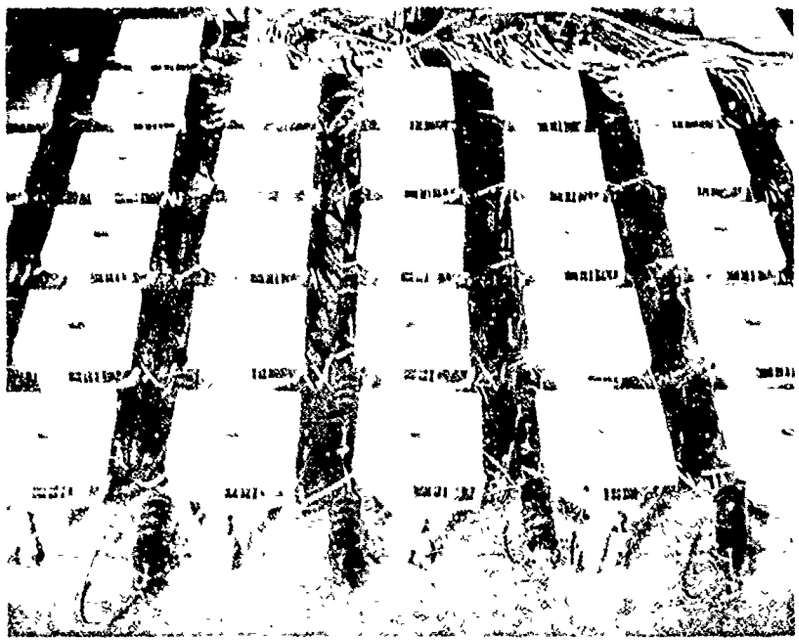


Figure 7. Typical Burn-in Rack

3.2 Burn-in Test Plan

The burn-in test plan shown in Figures 8, 9 and 10, was followed during the experimentation. The testing was divided into three parts, each designed to meet certain objectives as discussed in a latter section of the report. Since burn-in and electrical testing are so closely intertwined in the experimentation, they will be treated together in the chronological discussion of the experiment.

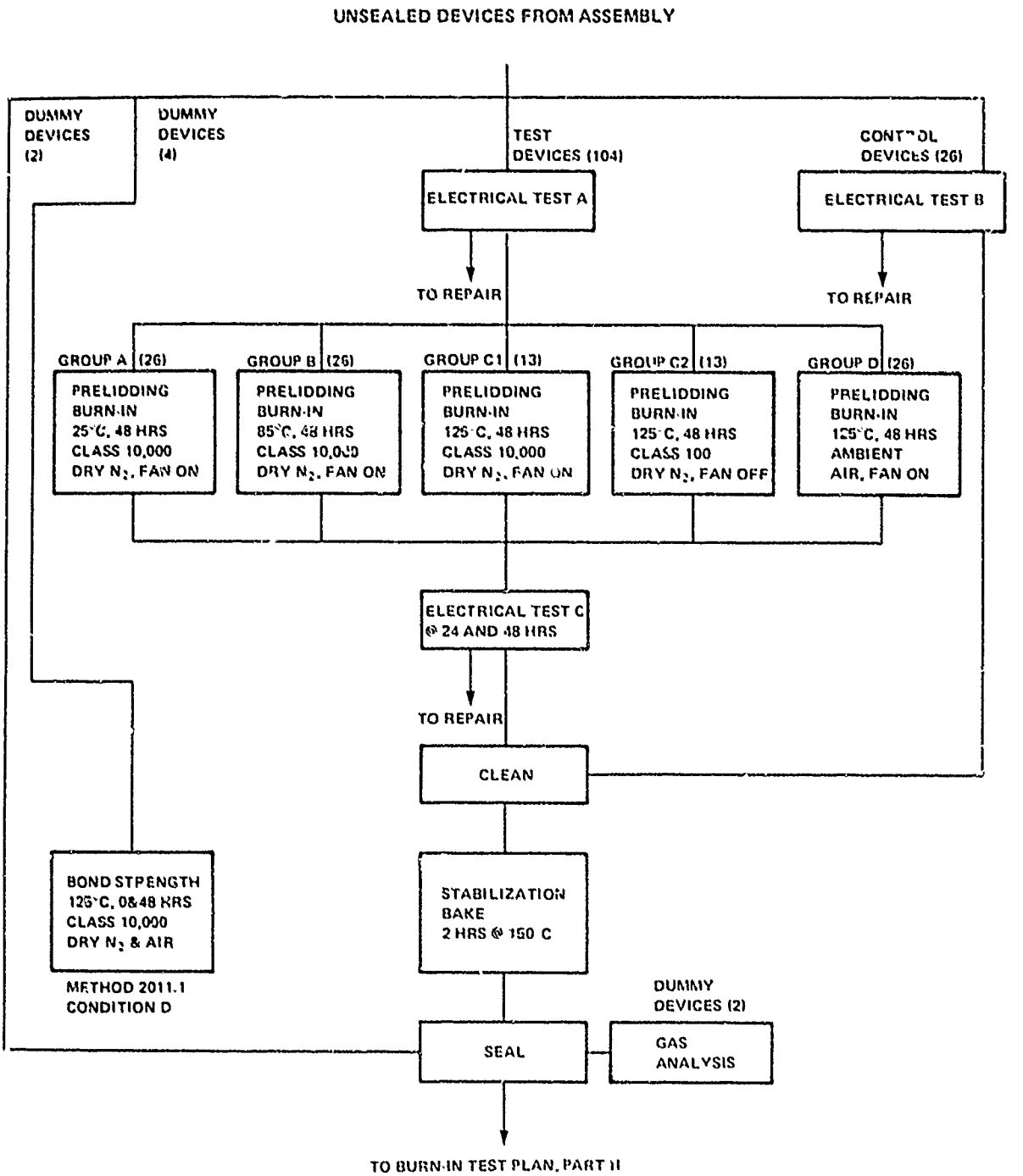


Figure 8. Burn-in Test Plan, Part I - Prelidding Burn-in

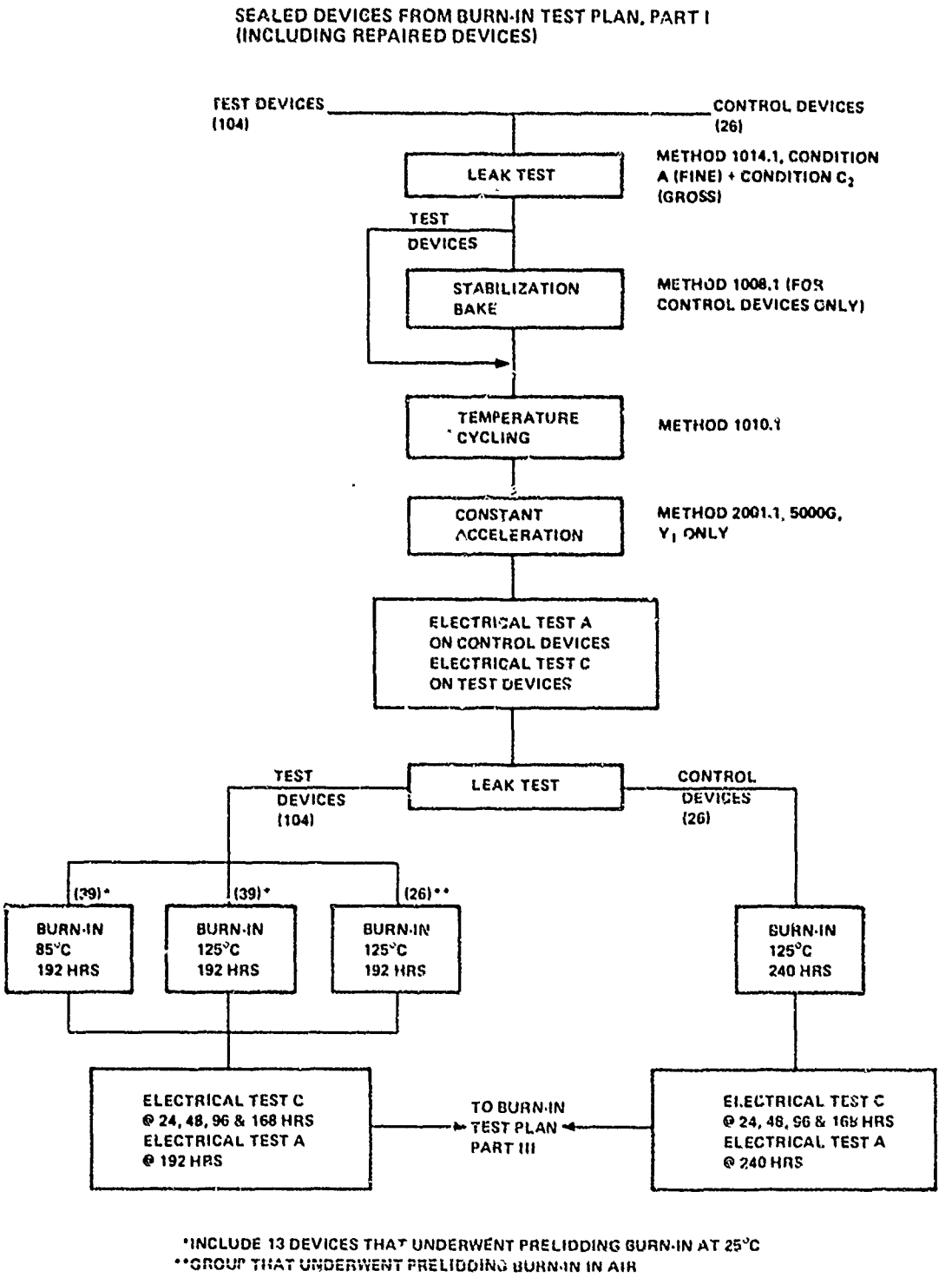
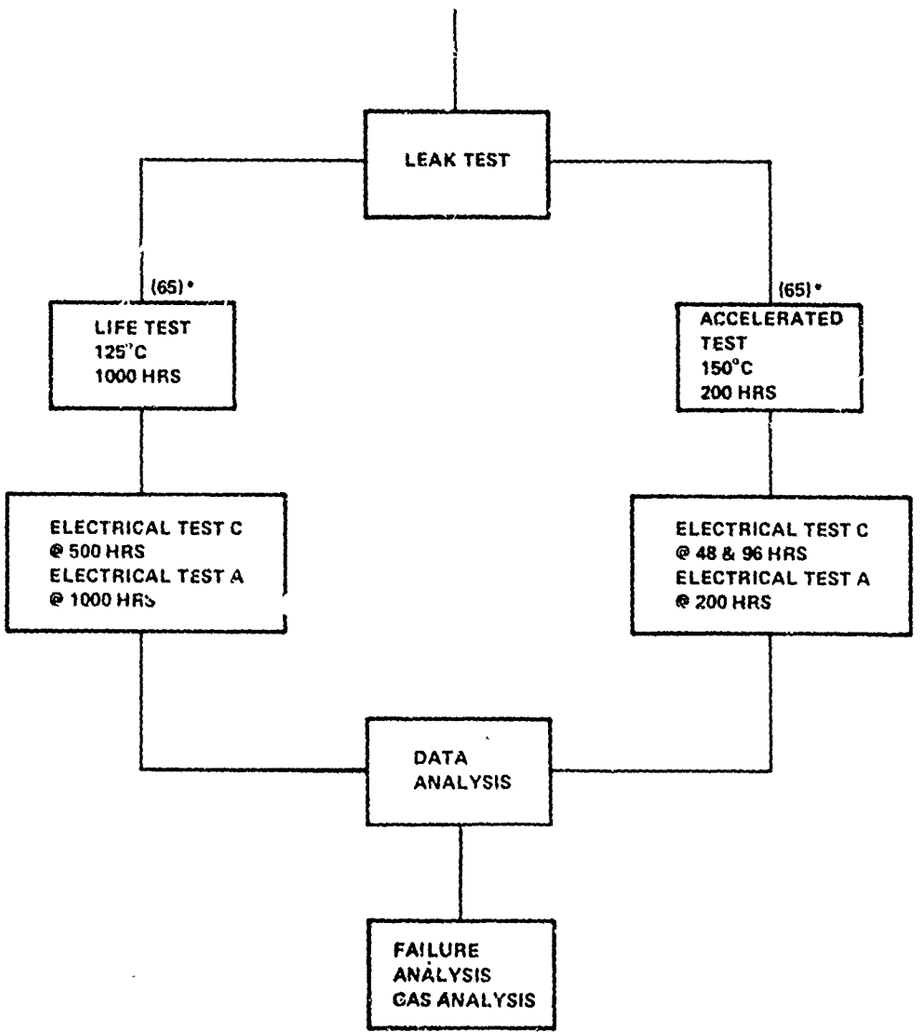


Figure 9. Burn-in Test Plan, Part II - Sealed Lid Burn-in

SEALED DEVICES FROM BURN-IN TEST PLAN, PART II



*52 TEST DEVICES AND 13 CONTROL DEVICES

Figure 10. Burn-in Test Plan, Part III - Life and Accelerated Testing

IV. ELECTRICAL TESTING

Electrical testing was performed at various points throughout the evaluation. At the chip level, 100% electrical testing at room temperature of all chip devices was performed utilizing a Teradyne J133 tester. After assembly operations were completed, devices were functionally tested using a specially constructed test box. Then, at the start of the experiment, baseline electrical testing at -55, 25 and 125°C was performed using a Macrodata 501 computerized test system which is shown in Figure 11. In order to facilitate testing of the hybrid circuit test vehicle, a special test

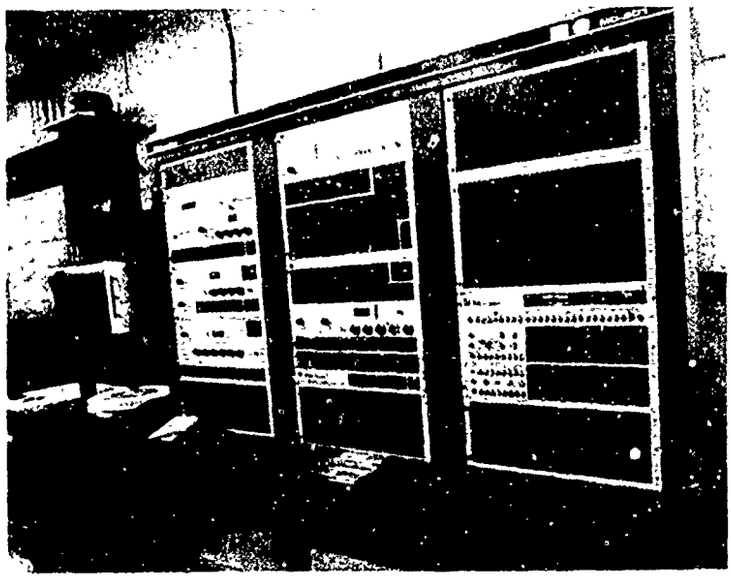


Figure 11. Macrodata 501 Test System

or load board shown in Figure 12, was built for the Macrodata 501 system that featured a zero insertion force socket. Use of this test board, with its gasketing and other features, greatly reduced the amount of time needed for the system to come to equilibrium at temperature extremes. A thermal environment chamber, which can be seen in Figure 11, was placed over this test board in which the device under test was mounted.

As can be seen in the test plan, at each electrical test point during the burn-in testing, different types of testing were specified. As shown in Table 3, this testing varied both in the temperature of performance and in the type of computer printout required. All test data, however, was

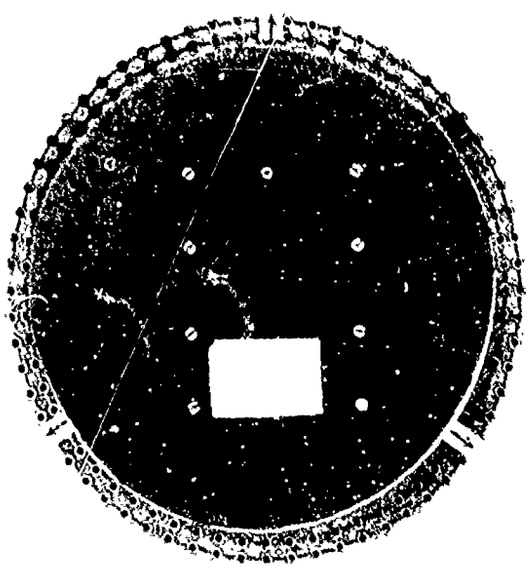


Figure 12. Macrodata 501 Test Board

stored on magnetic tape and could be retrieved as necessary. Regardless of the type of testing specified, each hybrid circuit test vehicle, at each electrical test point throughout the test plan, was tested for 51 functional and 62 parametric characteristics. This extensive amount of testing, which is detailed in Appendix B, was designed to fully electrically characterize each device in order to yield information useful in the performance of later rework, failure analysis, electrical data analysis and parametric shift analysis. In order to perform such a large amount of electrical testing, an extensive computer program was written for the Macrodata 501 system. A printout of the master program, along with a typical subroutine necessary to perform room temperature testing, is included in Appendix C.

TABLE 3

BURN-IN ELECTRICAL TESTING TYPES

Type of Testing	Temperature Points	Type of Printout
A	-55°C, 25°C and 125°C	All data
B	25°C	All data
C	25°C	Overlimit data only

V. EXPERIMENTATION

5.1 Experimental Objectives

The test plan which is shown in Figure 8, 9 and 10, and which should be referred to throughout the chronological discussion below for ease of understanding, was designed to answer questions posed in the Statement of Work. Specifically, the experiment was structured to:

1) determine if prelidding burn-in is effective.
2) determine if prelidding burn-in is non-destructive.
3) determine the optimum prelidding burn-in environment.
4) establish the optimum burn-in time duration and temperature before and after lidding.
5) establish temperature/time tradeoffs if appropriate.
6) evaluate the effect of the hybrid microcircuit rework that was accomplished during the experiment.
7) develop handling procedures to be used for prelidding burn-in.

5.2 Chronological Discussion of Experiment Results

Prior to the start of burn-in testing, all hybrid circuit test vehicles, which hereafter will be referred to as test or control devices, were marked with a unique code that described exactly what burn-in testing each test or control device would undergo. This code was stenciled on the cover of each device and the serial number was stenciled on the bottom of the package. Figure 5 shows the marking on a typical device. The 130 devices needed for the experimentation were ultimately broken down into 12 subgroups consisting of from six to 13 devices per group. The serial numbers, which ranged from 1 to 157, were assigned to devices in the order in which they were assembled. These devices were broken down into 12 subgroups in such a way as to assure that each subgroup contained devices covering the range of serial numbers. Each device was then stenciled with its unique six digit code. The first four digits identified the group the device was in

and the last two digits identified the device within that group. Devices were designated as test devices if they were to undergo prelidding burn-in; otherwise, they were designated as control devices. The five conditions of prelidding burn-in testing were coded, as were the two conditions of sealed lid burn-in testing and the two conditions of post burn-in testing. This corresponded to the Part I, II and III testing shown in the test plan. The coding system key is shown in Table 4. As an example, the device that was coded CO21-08, was a control device that, therefore, did not undergo prelidding burn-in but was sealed lid burned-in at 125 °C and then was exposed to life testing. It was the eighth device in its group.

TABLE 4

CODING SYSTEM KEY

Digit	Symbol	Explanation
First	C	Control device
	T	Test device
Second	0	No prelidding burn-in
	1	Prelidding burn-in at 25°C in nitrogen
	2	Prelidding burn-in at 85°C in nitrogen
	3	Prelidding burn-in at 125°C in nitrogen
	4	Prelidding burn-in at 125°C in air
Third	1	Sealed lid burn-in at 85°C
	2	Sealed lid burn-in at 125°C
Fourth	1	Life testing
	2	Accelerated testing
Fifth and Sixth	01 to 13	Device designation in group

Preliminary baseline electrical testing at room temperature was performed on all test and control devices, as well as on three devices that were designated as electrical standard devices. These standards were used at each electrical test point, prior to the start of testing, to assure that the computer program was working correctly. Data resulting from this testing

was used to set arbitrary test limits on the functional and parametric tests that are described in Appendix B. This testing also served to indicate those devices that were in need of minor rework. After this was completed, all devices were resubmitted for baseline electrical testing per the test plan in Figure 8. In the case of the test devices, testing was performed at -55, 25 and 125°C as indicated by electrical test Code A, which is explained in Table 3. Control devices were tested at room temperature only. Much longer times than expected were needed to reach stability at the temperature extremes, particularly at -55°C. Some condensation and frosting occurred which indicated that the environmental chamber was not tightly sealed to the test board. This problem was resolved by improving the gasketing on the test board, which is shown in Figure 12. As a result, test times at temperature extremes became more reasonable in length.

Prelidding burn-in was performed in one specially equipped oven as discussed earlier. Figure 13 shows typical unlidded devices mounted in a burn-in rack prior to the start of prelidding burn-in which was performed on the five groups of test devices in series.

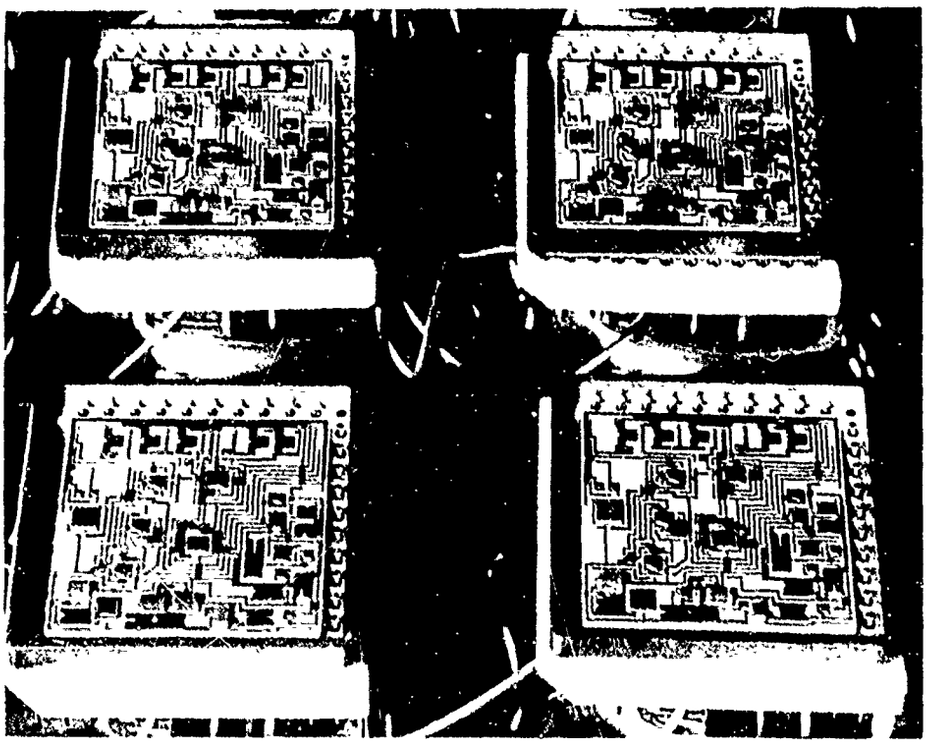


Figure 13. Typical Unlidded Test Devices Prior to the Start of Prelidding Burn-in

Electrical testing at room temperature was performed after 24 and 48 hours of prelidding burn-in. This testing revealed that nine devices had failed electrically after 24 hours of burn-in and one after 48 hours of burn-in as shown in Table 5. No failure analysis was performed per se on the ten failed devices; however, visual examination and pin to pin electrical probing revealed that six failures were caused by faulty burn-in rack wiring which

TABLE 5

PRELIDDING BURN-IN (PART I) FUNCTIONAL ELECTRICAL TEST RESULTS

Prelidding Burn-in Group*	Number of Devices	Functional Electrical Failures After 24 Hours		48 Hours	
		Burn-in	Other	Burn-in	Other
A(25°C, N_2)	26	[1]	3	0	0
B(85°C, N_2)	26	0	1	0	0
C1(125°C, N_2)	13	0	1	0	0
C2(125°C, N_2, fan off)	13	0	2	0	1
D(125°C, air)	26	0	1	0	0

Total Burn-in Failures - [1] or 0.96% (one device out of 104)

*See figure 8 for full identification of prelidding burn-in groups.

resulted in overstress and melting of bond wires. Three faults were caused by mishandling of the package lids. In order to protect the unlidded devices, it was decided to utilize the actual package lids which were kept in place with ordinary rubber bands. The lids were removed prior to insertion of devices into the burn-in sockets and replaced after the required prelidding burn-in had been completed and the devices had been removed from their sockets. In each of the three devices in question, a number of broken or

deformed wire bonds, which subsequently shorted, were observed. In each instance, the bonds along one edge of the device, in a regular straight line pattern, were damaged. Such damage could occur if the lid slipped into the package which, evidently, is what happened. An improved method of protection of unlidded devices is discussed in a later section of this report which is concerned with handling related failures. Only one failure, caused by a defective chip, can be considered a true burn-in related failure. This occurred on device T111-01 after 24 hours of prelidding burn-in at 25°C in dry nitrogen. The oven circulating fan was on which meant that particle count could have reached the 10,000 level. All ten devices were repaired and were returned to prelidding burn-in for an additional 48 hours. No additional failures occurred. The total failure percentage as a result of prelidding burn-in was 0.96% (one devices of 104). After all prelidding burn-in testing had been completed, all devices were cleaned, stabilization baked and then sealed. Two fully assembled but electrically non-functional dummy devices were also sealed and then sent to RADC for gas analysis. Results of these analyses, as well as gas analyses on devices that had undergone life testing, are discussed in a later section of this report. Four dummy devices were utilized for bond strength testing. Results of this testing are also discussed in a later section.

After sealing was completed, Part II of the test plan commenced. Fine and gross leak testing was performed on all devices. Fine leak testing was per Method 1014.1, Condition A of MIL-STD-883A except that devices were helium pressurized at ten psig for eight hours minimum rather than at 30 psig for four hours as specified. The reason for the change was that Raytheon, Quincy, had previous unsatisfactory results with this package when 30 psig was used; a high percentage of packages developed seam leaks after exposure to this pressure. In order to guard against this occurring in this experiment, it was decided to use the lower pressure and longer time; this was calculated to be equivalent to 30 psig for four hours. It was further decided that, at the end of the experiment, a representative number of devices would be tested at 30 psig for four hours to determine if seal damage would occur. After fine leak test had been completed, gross leak testing per Method 1014.1, Condition C2 per MIL-STD-883A was performed using

ten psig pressurization for 16 hr minimum. As a result of fine and gross leak testing, it was found that three devices had seal leaks and two had pin leaks. The three devices that had seal leaks were seam welded again which corrected the leaking. The two devices that had pin leaks, however, could not be repaired. It was decided not to remove these devices from the experiment because they were electrically functional. As testing progressed, these devices, and subsequent devices that developed pin leaks, were carefully watched for anomalous electrical behavior, but none occurred. Their performance is discussed in a later section of this report.

After leak testing, devices underwent the preconditioning shown in Figure 9. Stabilization bake was performed on the control devices only. Test devices bypassed this bake since thermal exposure, with resulting stressing, had already occurred during the prelidding burn-in testing. All devices were then temperature cycled and then subjected to constant acceleration testing. The substrate of one device, T111-03, separated from the package and, of course, was removed from the experiment. The remaining 129 devices underwent electrical testing with the control devices undergoing full baseline electrical testing, Code A, and the test devices undergoing Code C testing only. This revealed that 11 test devices and two control devices were functional electrical failures as shown in Table 6. The cause of these failures was later found to be broken wire bonds, primarily broken aluminum wire bonds which separated at the heel of the bond at the chip, or first bond, location. This is discussed in detail in a later section. These devices were distributed over all prelidding subgroups. Because of schedule considerations, it was decided not to repair these devices which were removed from the experiment. The total failure percentage of test devices, as a result of preconditioning, was 11.5% (12 devices out of 104); on control devices, this percentage was 5.4% (two devices out of 37). Leak testing was again performed on the 116 remaining devices; no new leak failures occurred. Sealed lid burn-in testing then commenced.

Two conditions of sealed lid burn-in were used on the test devices. The first was at 85°C for 192 hours and the second was at 125°C for 192 hours. Thirty-three test devices underwent burn-in at 85°C and 59 test devices underwent burn-in at 125°C. Twenty-four control devices were

TABLE 6

PRECONDITIONING (PART II) FUNCTIONAL ELECTRICAL TEST RESULTS

Prelidding Burn-in Group [a]	Number of Devices	Functional Electrical Failures After Preconditioning (Stabilization Bake, Thermal Cycling and Constant Acceleration)
A(25°C, N_2)	26	5 [b]
B(85°C, N_2)	26	2
C1(125°C, N_2)	13	1
C2(125°C, N_2 fan off)	13	2
D125°C, air)	26	2
Controls (original)	26	2
Controls (new)	11 [c]	0

Total Test Devices Failures - 12 or 11.5% (12 devices out of 104)

Total Control Device Failures - 2 or 5.4% (two devices out of 37)

Total Devices Remaining After Preconditioning - 127 (92 test and 35 control)

a) See figure 8 for full identification of prelidding burn-in groups.

b) Includes device with separated substrate.

c) This new group of controls was added to the experiment as a result of the loss of the original control group.

also burned-in at 125°C; however, these were scheduled to remain in burn-in for 240 hours. This longer length of time was to equalize the total burn-in time of all devices. Electrical testing C was performed on all devices after 24, 48, 96 and 168 hours. Electrical testing A was performed at the completion of sealed lid burn-in on all surviving test and control devices.

Electrical testing performed after the first 24 hour period of burn-in revealed that one control device had failed as shown in Table 7. This device was removed from the study, as were subsequent electrical failures, for delidding and visual and electrical examination. Because of schedule constraints, it was decided not to repair devices that failed during sealed lid burn-in. After 48 hours of burn-in, five additional devices had failed (four test and one control). Three more test devices failed at the 96 hour point and six more after 168 hours. After 192 hours, which was the full amount of sealed lid burn-in specified for test devices, no additional electrical failures occurred. A total of 13 test devices were removed from the experiment during Part II testing leaving 79 test devices for further testing. After 240 hours, which was the full amount of sealed lid burn-in specified for control devices, 22 electrical failures, or all of the control devices, occurred. This was caused by technician error. The control devices, which were being burned-in at 125°C, shared the same oven as the test devices. After the 79 test devices had been removed at the 192 hour point, the power supplies were not correctly set for the 48 hours of remaining burn-in on the control devices. This resulted in electrical overstress which caused extensive damage to all 22 control devices. A number of the damaged devices were opened and were observed to exhibit identical, extensive, and irrepairable damage.

TABLE 7

SEALED LID BURN-IN (PART II)
FUNCTIONAL ELECTRICAL TEST RESULTS

Prelidding Burn-in Group[a]	Number of Devices	Functional Electrical Failures After 24 Hours Burn-In	Other	48 Hours Burn-In	Other	96 Hours Burn-In	Other	168 Hours Burn-In	Other	192 Hours Burn-In	Other	240 Hours Burn-In	Other
A(25°C, N_2)	21	0	0	0	0	0	3	0	0	0	0	N. T.	
B(85°C, N_2)	24	0	0	0	1	0	0	0	2	0	0	N. T.	
C1(125°C, N_2)	12	0	0	0	0	0	0	[1]	1	0	0	N. T.	
C2(125°C, N_2, fan off)	11	0	0	[1]	1	0	0	0	0	0	0	N. T.	
D(125°C, air)	24	0	0	0	1	0	0	0	2	0	0	N. T.	
Controls (original)	24	(1)	0	0	1	0	0	0	0	0	0	0	22
Controls (new)	11	N. T.[b]		N. T.		N. T.		N. T.		N. T.		(1)	0

Total Test Device Burn-in Failures - [2] or 2.2% (two devices out of 92)

Total Control Device Burn-in Failures - (2) or 5.7% (two devices out of 35)

Total Devices Remaining After Sealed Lid Burn-in - 89 (79 test and 10 control)

[a] See Figure 8 for full identification of prelidding burn-in groups.

[b] N. T. = not tested

The 13 test devices that had failed during sealed lid burn-in were delidded. Visual examination and pin to pin electrical probing, coupled with Macrodata 501 electrical test data, revealed that 11 of the failures were handling related. Although it is not known specifically what occurred, the data suggests that these devices were incorrectly inserted into sockets. The device packages contained 30 pins distributed ten to a side on three sides, whereas, the burn-in sockets contained 40 pins distributed ten to a side on four sides. Only two of the failures can be considered to be true burn-in failures. Device T322-13, which failed after 48 hours of sealed lid-burn-in at 125 °C, was found to contain an oxide defect in component I1, which was a CD4007, CMOS digital IC. Device T321-09, which failed after 168 hr of sealed lid burn-in at 125 °C, was found to contain a defective 9LS112 LSTTL digital IC. This component, FF1, 2 appeared to have an etching defect. The total failure percentage of test devices, as a result of sealed lid burn-in, was 2. 2% (two devices out of 92).

The two control devices that had failed during sealed lid burn-in were delidded and examined as above. One failure was considered to be handling related as discussed above; however, device CO22-07 was found to have a diffusion defect in component IC4, which was a CD4007 CMOS digital IC. This device failed after 24 hr of burn-in. The total failure percentage of the original control devices as a result of sealed lid burn-in was 4. 2% (one device out of 24). This figure increased to 5. 7% (two devices out of 35) when an additional failure from the new control group was factored in as is discussed below.

Although only 130 devices were needed for burn-in testing, enough material was purchased to fabricate approximately 157 devices. None of these 27 extra devices, most of which were unsealed, had undergone any kind of burn-in. Some of these devices had been designated for specific purposes such as bond strength testing, gas analysis, electrical standards, etc. Of the devices available, a new control group of 11 devices was formed. These devices, which were identified only by their serial numbers, underwent baseline electrical testing at room temperature and were found to be acceptable. Leak testing was then performed.

This showed that six of the devices had pin leaks. It was decided, however, to proceed with these devices because they were acceptable electrically and because the two earlier test devices that had pin leaks had successfully completed sealed lid burn-in testing. As with the two earlier pin leak test devices, these six new pin leak control devices were carefully watched for anomalous electrical behavior. None occurred as is discussed later. All 11 new control devices then underwent the preconditioning and electrical testing A prescribed by the test plan. Results of this electrical testing compared favorably with results on the original 26 control devices. Leak testing revealed that no additional devices had lost hermeticity. Since electrical test data existed on the original control devices at 24, 48, 96 and 168 hr, and since remaining evaluation time was limited, it was decided to expose the 11 new control devices to 240 hr of uninterrupted sealed lid burn-in testing at 125 °C followed by electrical testing. One device, serial number 146, was a functional failure. This device was removed from the experiment, delidded and examined. Component 11, which was a CD4007 CMOS digital IC, contained a degraded gate. This failure, added to the one previously found in the original control group, caused the failure percentage of all control devices, as a result of sealed lid burn-in, to rise to 5.7% (two devices out of 35). This is in contrast to the failure percentage of 2.2% (two devices out of 92) observed in the test devices that had undergone sealed lid burn-in. A total of 25 control devices were removed from the experiment during Part II testing leaving ten control devices for further testing.

While the new group of control devices was being preconditioned and sealed lid burned-in, the 79 surviving test devices were leak tested. They successfully passed this. Forty-two devices were then committed to life testing at 125 °C for 1,500 hr as shown in Figure 10. The remaining 37 test devices were earmarked for accelerated testing at 150 °C for 200 hr; however, the start of this testing was delayed until the new control devices were ready. Five of the new control devices were earmarked for accelerated testing and the other five for life testing. Because of the delay which resulted from the demise of the original control devices, the new control devices would ultimately undergo only 1,000 hr of life testing.

Electrical testing was performed on test devices after 500, 1000, and 1,500 hr of life testing. One test device, T211-13 which had been prelid and sealed lid burned-in at 85°C in nitrogen, failed functionally after 500 hr of testing as shown in Table 8. Failure analysis was performed on this device and is discussed in detail in a later section of this report. No failures occurred after 1,000 and 1,500 hr of life testing. As shown in Table 8 one test device failed as a result of life testing or 2.4% (one device out of 42). The control devices joined the test devices already in life testing; no failures occurred in these devices after 500 and 1,000 hr of life testing.

TABLE 8

LIFE TESTING (PART III)
FUNCTIONAL ELECTRICAL TEST RESULTS

Prelidding Burn-In Group[a]	Number of Devices	Functional Electrical Failures After 500 Hours Burn-In	500 Hours Other	1000 Hours Burn-In	1000 Hours Other	1500 Hours Burn-In	1500 Hours Other
A(25°C, N_2)	10	0	0	0	0	0	0
B(85°C, N_2)	11	[1]	0	0	0	0	0
C1(125°C, N_2)	5	0	0	0	0	0	0
C2(125°C, N_2, fan off)	4	0	0	0	0	0	0
D(125°C, air)	12	0	0	0	0	0	0
Controls (new)	5	0	0	0	0	N. T.[b]	

Total Test Device Burn-In Failures - [1] or 2.4% (one device out of 42)

Total Control Device Burn-In Failures - 0

[a] See Figure 8 for full identification of prelidding burn-in groups.

[b] N. T. = not tested

Five of the new control devices and the 37 remaining test devices successfully underwent accelerated testing. Electrical testing was performed on all devices after 48 and 200 hr of accelerated testing and no functional failure was found as shown in Table 9. These devices were also scheduled to be electrically tested after 96 hr of accelerated testing; however, a plant shutdown, as a result of a severe snow storm, caused that test point to be missed.

It should be noted that all electrical failures that occurred throughout the experiment, which led to removal of the failed devices from the experiment, were functional failures. No attempt was made to cull out those devices that exhibited parametric shift. This was deliberately done because it was desired to learn if devices from any one of the prelidding burn-in subgroups would exhibit a higher degree of parametric shift than would others at the end of life and accelerated testing. As will be seen in the experimental results discussion below, parametric shifts did occur but were not exclusively associated with any one prelidding burn-in subgroup.

TABLE 9

ACCELERATED TESTING (PART III)
FUNCTIONAL ELECTRICAL TEST RESULTS

Prelidding Burn-In Group[a]	Number of Devices	Functional Electrical Failures After 48 Hours Burn-In	Other	200 Hours Burn-In	Other
A(25 °C, N_2)	8	0	0	0	0
B(85 °C, N_2)	10	0	0	0	0
C1(125 °C, N_2)	5	0	0	0	0
C2(125 °C, N_2, fan off)	5	0	0	0	0
D(125 °C, air)	9	0	0	0	0
Controls (new)	5	0	0	0	0

Total Test Device Burn-In Failures - 0
Total Control Device Burn-In Failures - 0

[a] See Figure 8 for full identification of prelidding burn-in groups.

VI. EXPERIMENTAL RESULTS

6.1 Data Analysis Methodology

Of the 141 devices that were involved in the main thrust of the experiment, 88 remained after all testing had been completed. Fifty-three devices had been removed from the experiment. Only five of these were functional electrical failures. The rest failed because of technician error (22 devices), preconditioning related damage (14 devices) and handling errors (12 devices).

A massive amount of parametric electrical test data had been generated on the forty-one test devices and five control devices that had completed life testing and the 37 test devices and five control devices that had completed accelerated testing without functional electrical failure. At each electrical test point through the experiment, each device had undergone 62 parametric tests. It was decided to first analyze the end point parametric data. Accelerated testing data was examined first since this testing was expected to provide the most stress on the devices because of the higher testing temperatures and thus result in a greater number of parametric shifts. Then life testing data was examined. It was decided to designate the 1,000 hour test device life test data as the end point data, even though 1,500 hour data existed, because the new control devices had only undergone 1,000 hours of life testing. The 1,500 hour test device life test data, however, was considered in the parametric shift analysis.

Histograms were generated for each of the 62 parametric tests for all devices that had undergone accelerated testing. This graphically showed the distribution of the test values and revealed those devices that had values for that particular test outside of the test limits. These test limits were set based upon the distribution of test values that occurred on all devices during preliminary baseline electrical testing, and on the allowable operating range permitted by the circuit design. These histograms were then compared with histograms showing the distribution

of initial test values for the parametric test in question for all test and control devices. The out-of-limit end point test values were then checked against initial out-of-limit data. If no initial out-of-limit data existed, then all of the devices that contained out-of-limit end point data were considered to be failures. The purpose of these comparisons, more simply stated, was to avoid assessing parametric failures that existed at the start of the experiment as parametric failures that occurred as a result of the experiment. Only a few initial parametric failures were isolated and these were factored out of the analysis.

This same approach was used to analyze 1,000 hour life test data to determine parametric failures. Also, where considered appropriate, additional histograms were generated to display data after 168 hours of sealed lid burn-in. The 168 hour point was chosen because it was the last point where data was collected on the 22 original control devices before they were damaged and removed from the experiment. To gain more information relative to the onset of parametric shift, all failed parametric tests in the test devices were traced back to the point where shift started. This will be shown in tabular form in the next section

To illustrate this data analysis approach, a series of histograms will now be presented. These are of parametric test 7 which measured the V_{OL} (voltage output low) of component IC4 which is a CMOS digital IC, CD4007. For simplicity, room temperature baseline data will be presented first, followed by 168 hour sealed lid burn-in data, 1,000 hour life test data and 200 hour accelerated data. These will be followed by similar histograms of parametric test data collected at -55 and +125°. It should be noted that the number of devices represented in the histograms necessarily varies. This reflects the various subgroups shown in Figures 7, 8 and 9 and the removal of devices from the study as mentioned in the previous chronological discussion.

Figure 14 shows the room temperature initial parametric test results for test 7. It can be seen that all but one of the devices had test values within the 0 to 20 mV test limits and that three of the devices were separate from the main distribution. The one device (T211-08) that was outside of the test limit was considered to be a parametric failure. The histogram was constructed to show the percentage of devices in each cell interval, which, in this case was 1 mV.

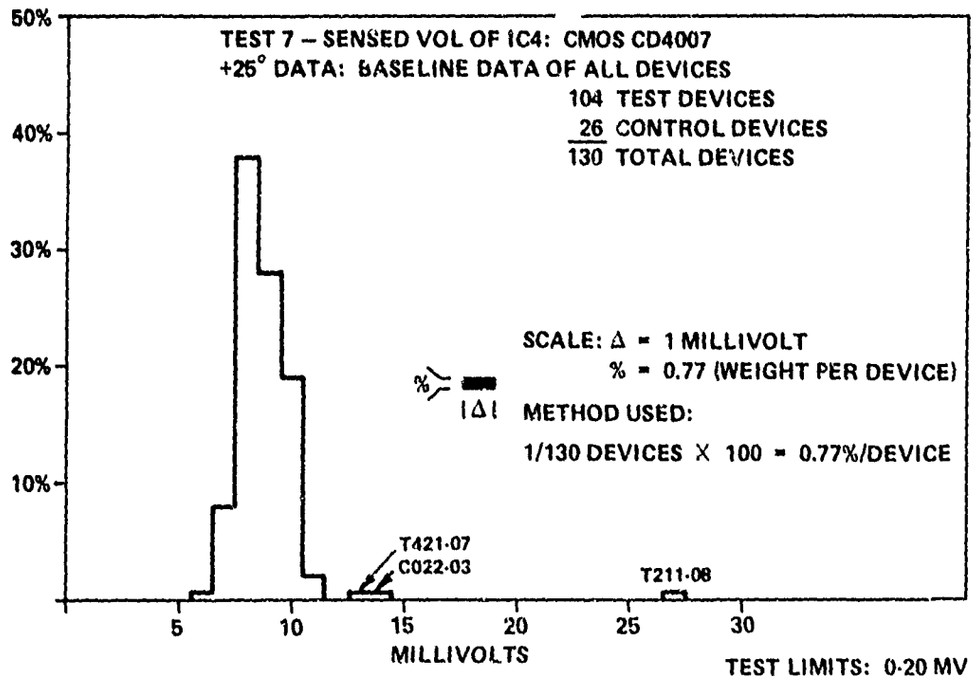


FIGURE 14. TEST 7, BASELINE 25°C DATA

Figure 14. Test 7, Initial 25 °C Data

Figure 15 shows the distribution of test values after 168 hours of sealed burn-in at 125 °C for 32 test devices. Note that two devices were outside of the test limits. Figure 16 shows 168 hour data for 22 control devices which had not been exposed to prelidding burn-in. Note that parametric shift has occurred to a lesser extent than in the test devices.

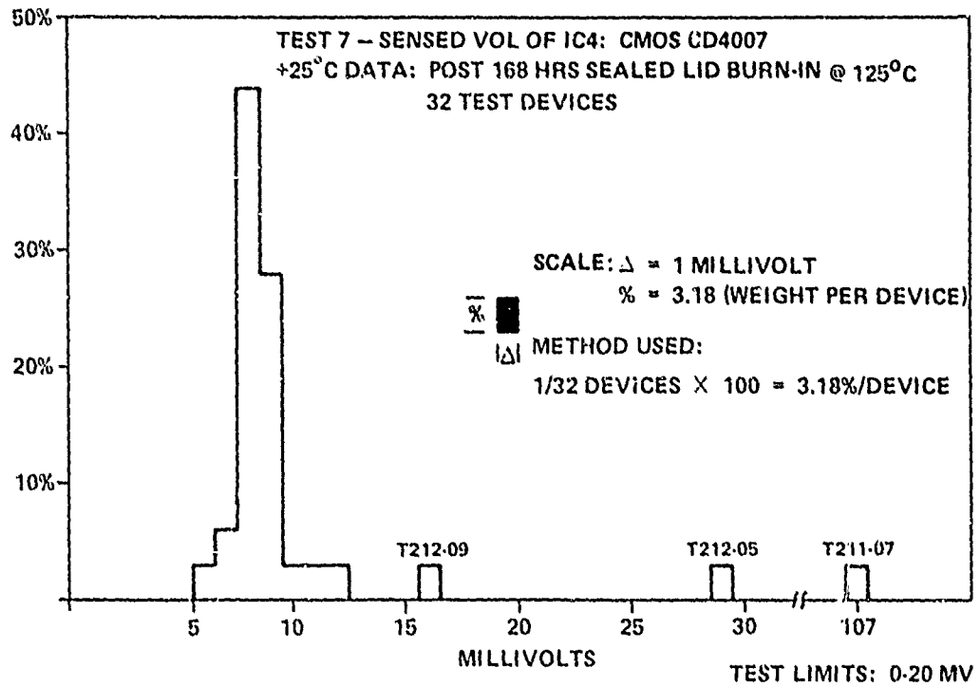


Figure 15. Test 7, Post 168 Hours at 125 °C Data on Test Devices (25 °C)

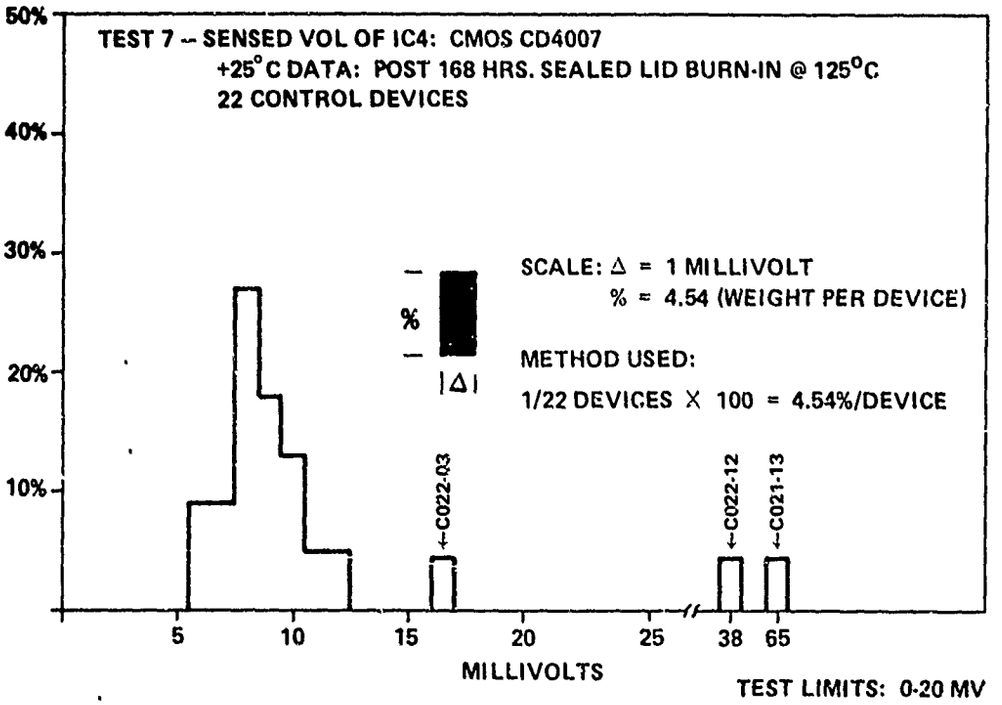


Figure 16 - Test 7, Post 168 Hr at 125°C Data on Controls (25°C)

Figure 17 shows 1,000 hr life test data for 41 test devices. Note that three devices were beyond the test limit and were therefore parametric failures. Figure 18 shows 1000 hr life test data for five control devices. No devices shifted beyond the test limit.

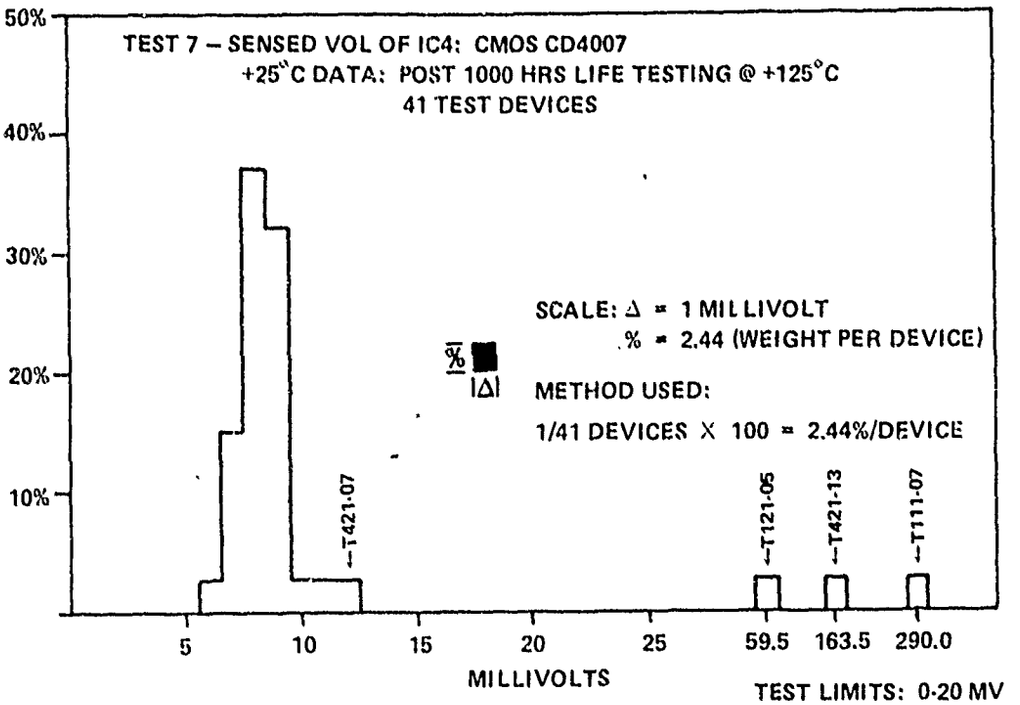


Figure 17 - Test 7, Post 1000 Hr at 125°C Data on Test Devices (25°C)

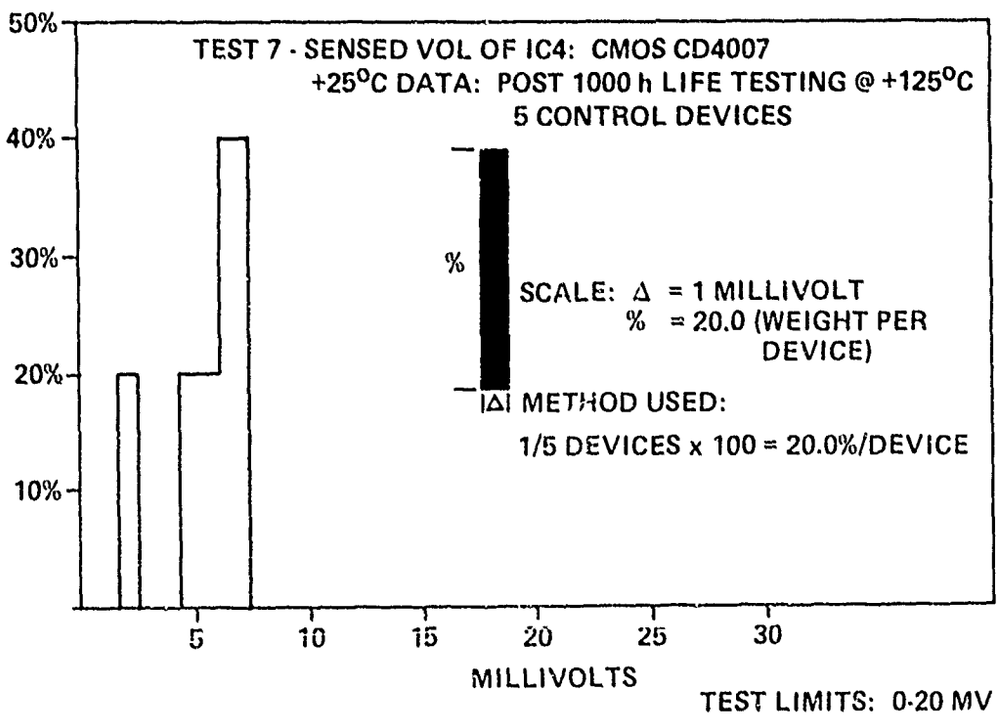


Figure 18 - Test 7, Post 1000 Hr at 125°C Data on Control Devices (25°C)

Figure 19 shows 200 hr accelerated test data for 37 test devices. Note that eight devices shifted beyond the test limit and were parametric failures. Figure 20 shows 200 hr accelerated test data for five control devices. One device is a parametric failure.

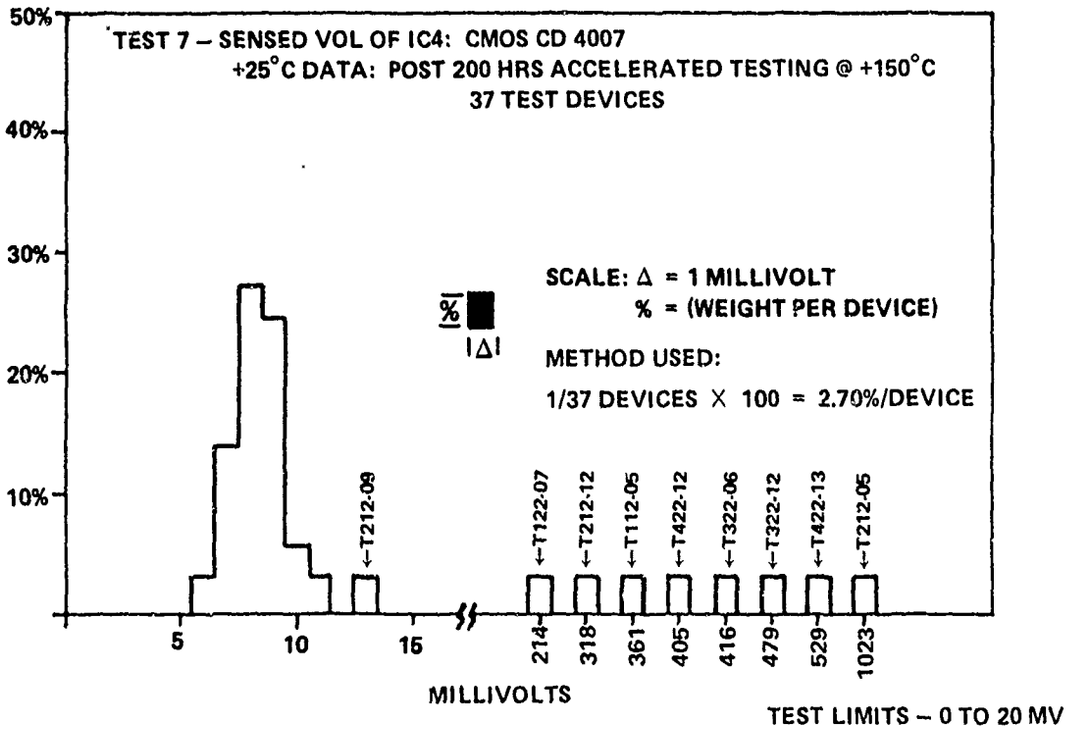


Figure 19 - Test 7, Post 200 Hr at 150°C Data on Test Devices (25°C)

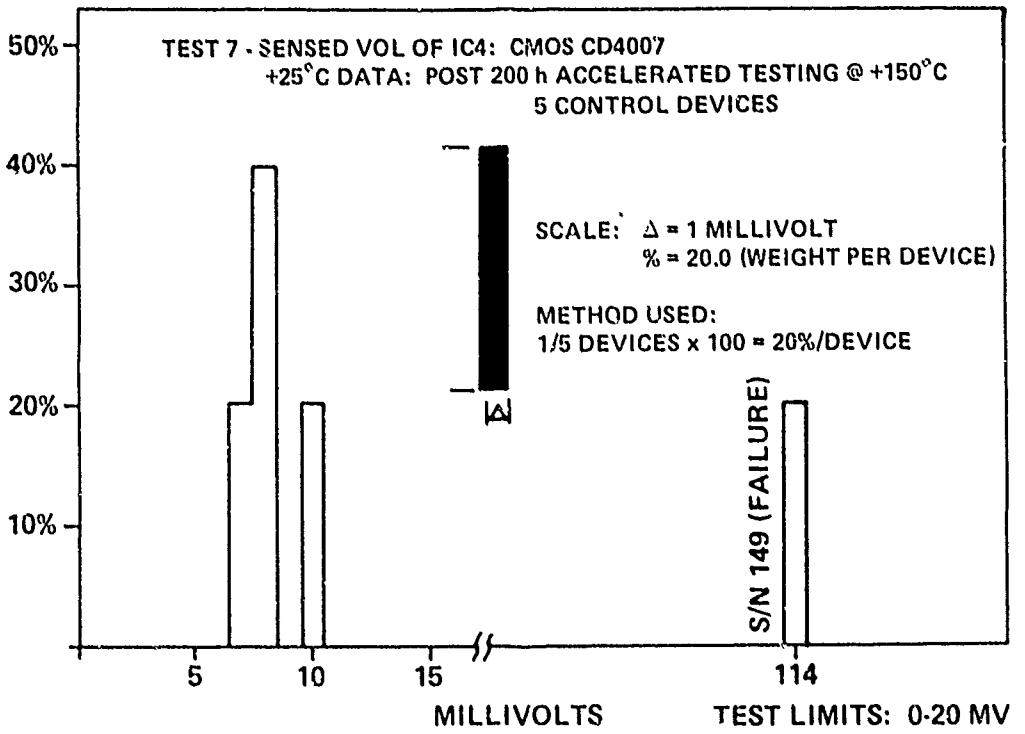


Figure 20 - Test 7, Post 200 Hr at 150°C Data on Control Devices (25°C)

Figure 21 shows initial data taken at -55°C. Two devices were beyond the test limits. One device, T111-01, failed functionally after 24 hr of prelidding burn-in at 25°C and was repaired. Figure 22 shows 1,000 hr life test data taken at -55°C for 41 test and five control devices. Note that three devices were failures.

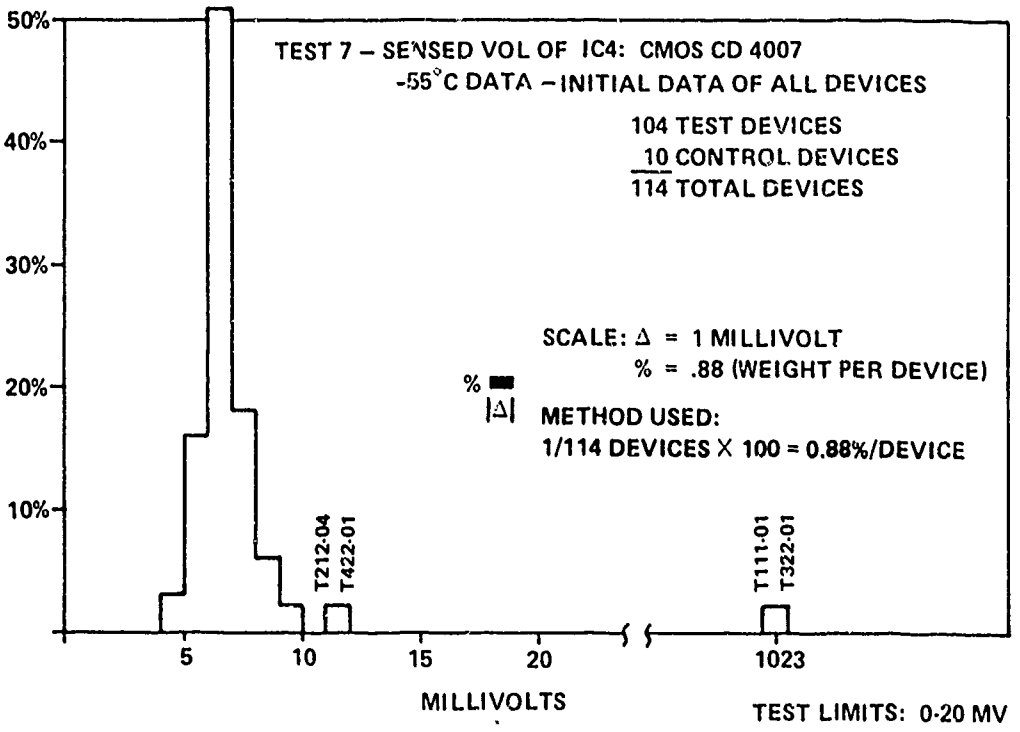


Figure 21 - Test 7, Initial -55°C Data

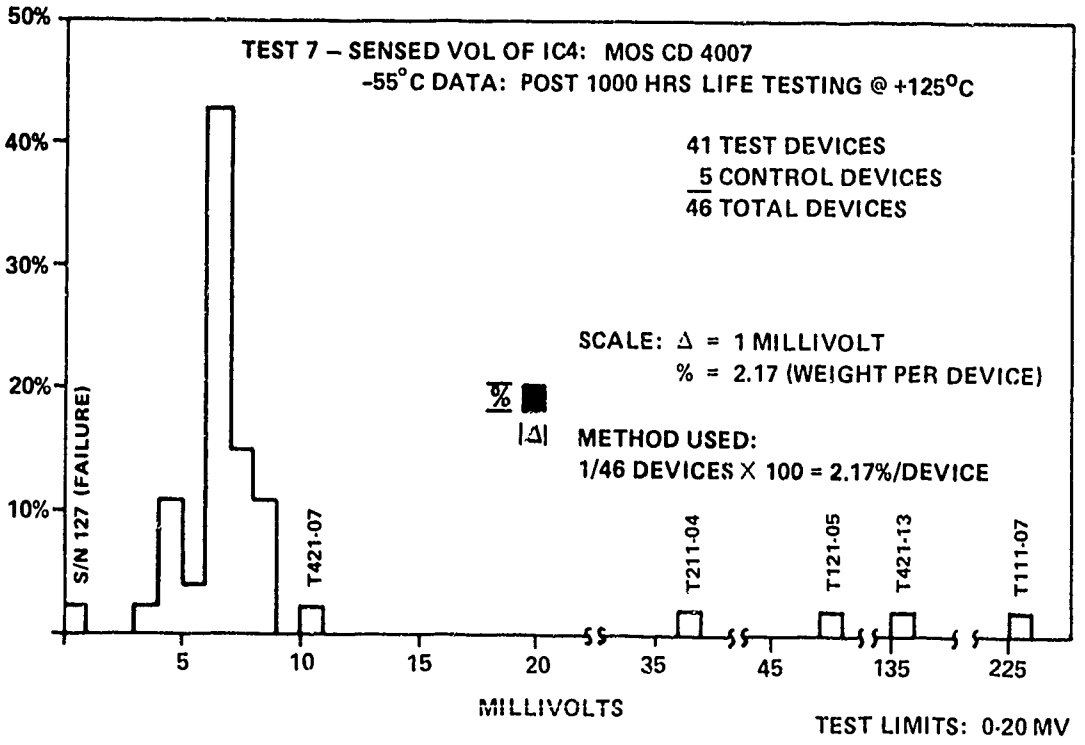


Figure 22 - Test 7, Post 1000 Hr at 125°C Data (-55°C)

Figure 23 shows baseline data taken at +125°C; two devices failed. Figure 24 shows 1,000 hr life test data for 41 test and five control devices; three devices failed.

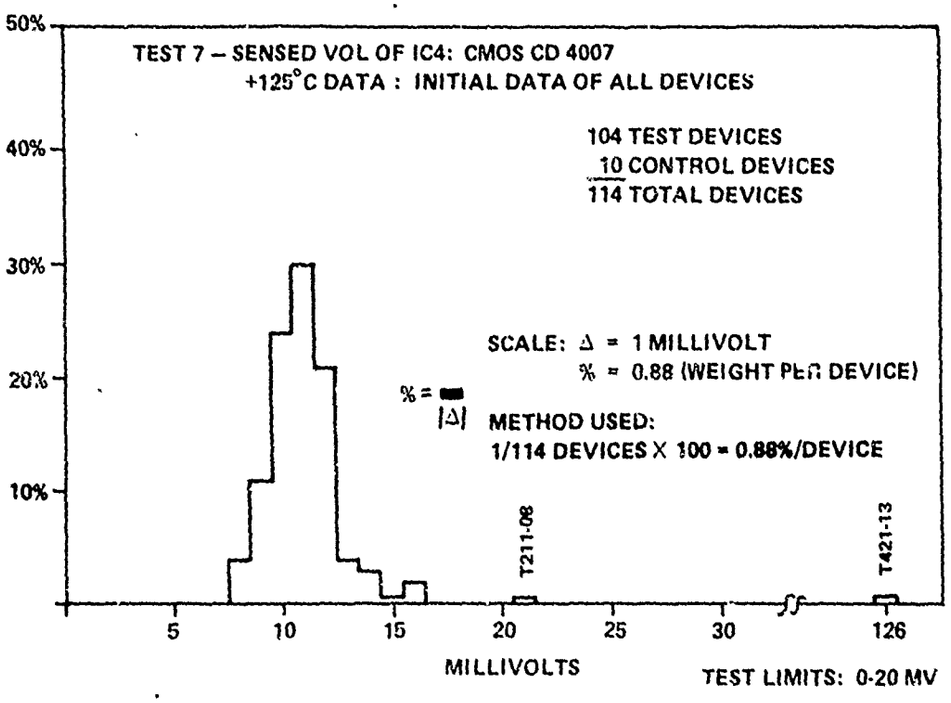


Figure 23 - Test 7, Initial 125°C Data

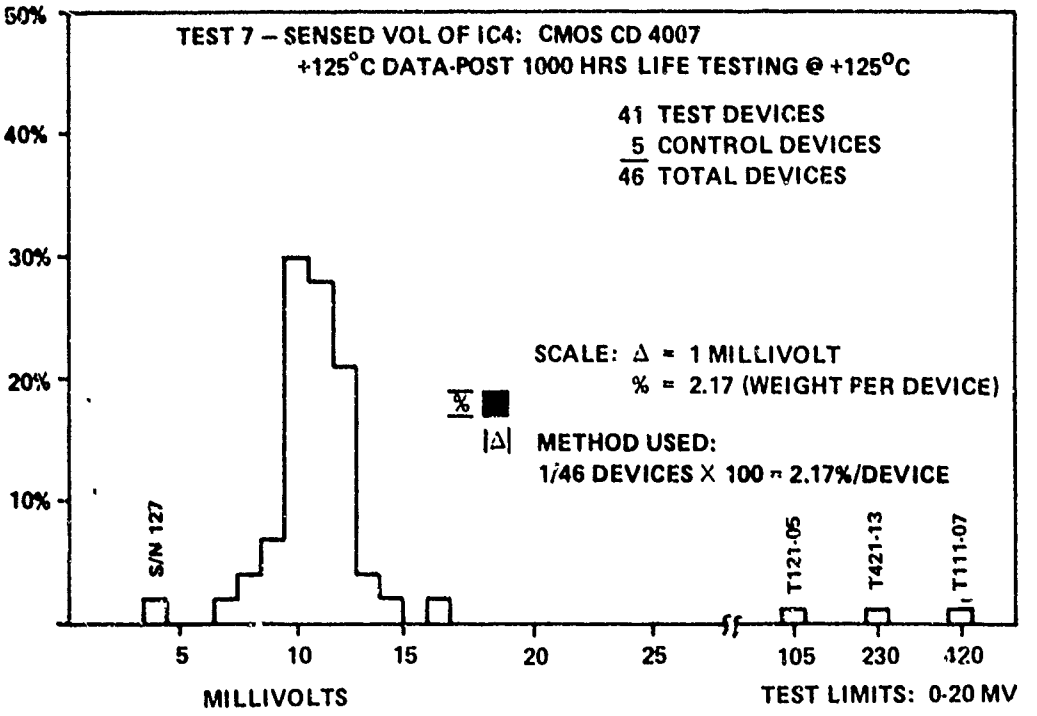


Figure 24 - Test 7, Post 1000 Hr at 125°C Data (+125°C)

Histograms of other parametric tests are included in Appendix D. These were picked to be representative of the various component types used in the device. These histograms revealed that, while some parametric shift did occur on some components, none can compare to the amount of shift that occurred on the CMOS ICs as shown in the test 7 histograms. Shift was not restricted to test devices only; control devices also shifted. This demonstrated that parametric shift was not exclusively associated with devices that had undergone prelidding burn-in. The Schottky diodes, the diffused diodes, the LM139 comparators, and the JFET transistors were stable. Some shift occurred in the LSTTL ICs; however, only one device exceeded test limits after life testing. Less shift occurred in thick film resistors after life testing than before. The thin film resistors in one device shifted beyond test limits after life testing.

Since this experiment was not primarily concerned with parametric shifts of components as a function of burn-in exposure, no attempt will be made to analyze or explain this data further.

6.2 Discussion of Results

As a result of the parametric data analysis performed above, end-point life test and accelerated parametric test failures could be identified for test and control devices. A failure occurred when a given parameter shifted outside of its test limits. In some instances, a considerable amount of shift away from the massed central distribution of test results occurred for a particular device but the end-point value was within the test limits. Test results such as these were not considered to be failures. As can be seen in Table 10, parametric failure percentage for test devices after 1,000 hr of life testing at 125°C compared very favorably with the failure percentage for control devices (14.3% versus 20.0%).

At first glance, the failure percentage for group C2 appeared to be attractively low. This group was burned-in in dry nitrogen without the oven circulating fan running. This meant that a Class 100 environment existed. This test group consisted of only four devices. All other groups run in nitrogen with the fan on, or in a Class 10,000 maximum environment, had failure percentages similar to or less than the control devices. These facts make the Group C2 failure percentage result less compelling. A Class 10,000 maximum environment is probably the best that can be hoped for using standard burn-in ovens operating in a normal (or fan on) mode.

The life test failure percentage for devices pre-lid burned-in in air was slightly higher than that for devices prelid burned-in in nitrogen (16.7% versus 13.8%). Based on this, it is felt that prelidding burn-in in nitrogen is preferable.

After the 1,000 hr life test parametric failures were identified, it was desired to determine at what point parametric shift started to occur in the six failed test devices and one failed control device. Table 11 is an analysis of shift data. Three sealed lid burn-in data points (24, 48, and 192 hr) and three life test data points (500, 1,000, and 1,500 hr) are included. The data shows, generally, that shift started in the first 500 hr of life testing. In a few tests, shift started during sealed lid burn-in; however, no shift occurred during prelidding burn-in.

TABLE 10

LIFE TESTING (PART III)
PARAMETRIC ELECTRICAL TEST RESULTS

Prelidding Burn-in Group [a]	Number of Devices	Parametric Electrical Failures After 500 Hours	1000 Hours	1500 Hours
A(25°C, N_2)	10	0	2	0
B(85°C, N_2)	11	0	1	0
C1(125°C, N_2)	5	0	1	0
C2(125°C, N_2, fan off)	4	0	0	0
D(125°C, air)	12	0	2	0
Controls (new)	5	0	1	N. T. [b]

Total Test Device Failures - 6 or 14.3% (six devices out of 42)

Total Control Device Failures - 1 or 20.0% (one device out of five)

a) See Figure 8 for full identification of prelidding burn-in groups.

b) N. T. = not tested

TABLE 11

PARAMETRIC SHIFT ANALYSIS

Device	Test No.[a]	Initial Data	After Sealed Lid Burn-in 24 hrs	48 hrs	192 hrs	After Life Testing 500 hrs	1000 hrs	1500 hrs
T111-07	2	1.225	1.220	1.215	1.220	1.150	1.045[b]	960
	7	7.5	7	9	8	192	290	404
	16	5.005	5.005	5.010	5.005	5.005	4.460	3.180
T121-05	2	1.235	1.220	1.230	1.195	755	780	945
	3	1.060	1.050	1.050	1.065	725	780	990
	7	9	7	8	14	88	59.5	52
	8	5.005	5.005	5.005	5.005	260	205	260
	15	9	11	8	12	18.5	17	12.5
	16	5.005	4.950	5.005	4.790	15	15	10
	57	-0.373	-0.371	-0.373	-0.357	-21	-23.5	-37
T211-10	41	214	214	212	214	213	669.5	336
T321-11	15	9	10	10	11	23.5	25.5	22
	16	5.005	5.005	4.965	4.815	3.210	3.185	2.380
T421-12	31	22.150	22.000	22.000	21.700	22.000	2.050	2.050
	33	4.275	4.275	4.275	4.275	4.275	150	160
T421-13	7	10	9	10	8	39	163.5	340
	15	8.5	9	9	10	24.5	28	27.5
	16	5.005	4.990	4.995	4.870	2.705	2.855	2.365
#127	26	0.659	0.659	0.660	N.T.[c]	0.656	1.023	N.T.

a) See Appendix B for test details.

b) Underline indicates first shift beyond test limits.

c) N.T. = not tested.

As shown in Table 12, the parametric failure percentage for test devices after 200 hr of accelerated testing at 150°C was higher than for the control devices, but not substantially so (67.6% versus 60.0%).

When compared with the functional electrical test failure percentages (Tables 8 and 9), parametric test failure percentages (Tables 10 and 12) of test and control devices, after life and especially after accelerated testing, appear high. This suggests that the parametric test limits were too tightly set.

TABLE 12

ACCELERATED TESTING (PART III)
PARAMETRIC ELECTRICAL TEST RESULTS

Prelidding Burn-in Group [a]	Number of Devices	Parametric Electrical Failures After 48 Hours	Parametric Electrical Failures After 200 Hours
A(25°C, N_2)	8	0	4
B(85°C, N_2)	10	0	8
C1(125°C, N_2)	5	0	4
C2(125°C, N_2, fan off)	5	0	4
D(125°C, air)	9	0	5
Controls (new)	5	0	3

Total Test Device Failures - 25 or 67.6% (25 devices out of 37)
Total Control Device Failures - 3 or 60.0% (three devices out of five)

a) See Figure 8 for full identification of prelidding burn-in groups.

Results of prelidding burn-in and sealed lid burn-in were presented in a previous section of this report. As was shown earlier in Table 5, only one functional failure occurred during prelidding burn-in and that was during the first 24 hr at 25°C (Group A). Life testing results have shown that an air environment is not as desirable as a dry nitrogen environment in terms of parametric shift. Life and accelerated testing results have shown also that prelidding burn-in at 125°C had no apparent ill effect. It is felt that the highest stress possible should be applied to devices during prelidding burn-in since this has the greatest potential to weed out defective devices. This points to a prelidding burn-in temperature of 125°C as being optimum. Although no functional failure occurred in prelidding burn-in beyond 24 hr, no apparent ill effect was noted in the devices prelid burned-in for 48 hr. On the premise that the longer that the stress (temperature) is applied, the greater is the potential for identifying defective devices, it appears that the appropriate length of prelidding burn-in should be 48 hr.

Sealed lid burn-in failure percentages were shown earlier in Table 7. As would be expected, the failure percentage for devices that were prelid burned-in was lower than for devices, the controls, that were not. This is an indication that prelidding burn-in is effective. Since all of the test device failures occurred at 125°C, this temperature is considered optimum for sealed lid burn-in.

The effect of prelidding burn-in on preconditioning failures was shown earlier in Table 6. As was seen, the failure percentage for test devices was more than twice that for control devices (11.5% versus 5.4%). Of the 14 devices that failed after preconditioning, 12 were test devices and two were controls. In one of the 12 test devices, the substrate separated from the package after constant acceleration; however, the reason for failure of the remaining 11 test devices, as well as the two control devices, was not apparent until the devices were opened and examined. All of the devices contained broken wires. Of the 11 test devices, three had broken gold bond wires. The remaining eight test devices had broken aluminum bond wires. Both of the control devices had broken aluminum bond wires. Almost all of the wires, both gold and aluminum, broke at the heel of the first bond, or the bond at the chip. This is shown in Figure 25 which is a scanning electron microscope (SEM) photograph of a typical ultrasonic aluminum wire bond failure.

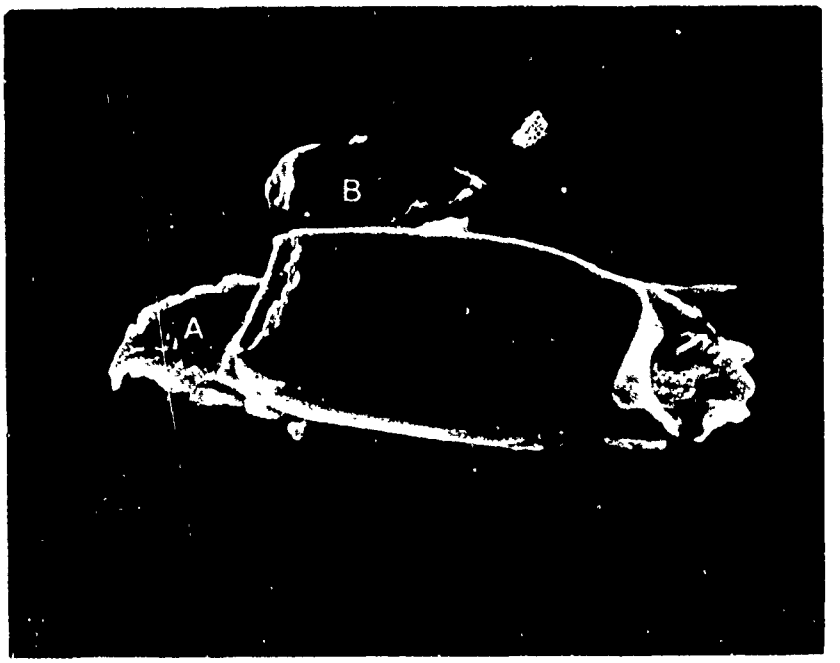


Figure 25 - Scanning Electron Microscope (SEM)
Photograph of a Typical Ultrasonic Aluminum Wire Bond Failure,
550X Magnification

The 1 mil diameter aluminum wire used in all of the devices in the experiment had an 18 to 22 gram tensile strength. All of the bonds were made by the same operator using the same piece of equipment at Raytheon, Quincy. This location no longer uses this wire and has changed to the less brittle 16 to 18 gram tensile strength type. As can be seen in Figure 25, the foot of the bond is approximately two mils, or two wire diameters, wide. While this is within the MIL-STD-883 allowances, it is considered to be excessively wide for 18 to 22 gram tensile strength wire. Based on this, it is felt that too much pressure was used during the bonding operation which resulted in weakening of the bond at the heel. Failure of the bonds so weakened probably occurred during the thermal cycling portion of pre-conditioning. X-ray energy spectrographic (XES) analysis was performed in the areas labeled A and B in Figure 25. This revealed the presence of aluminum only. Area A is the tail of a previous ultrasonic wire bond.

Area B is a probe mark caused by the electrical testing of the chip prior to assembly. Nondestructive wire bond pull testing was performed on a number of wire bonds adjacent to failed wire bonds in three devices. All of these bonds survived a three gram pull. None of these bonds exhibited any notching or ultrasonic tool related defect in the heel area. All of them, however, did have approximately two mil wide feet. It is not understood why these bonds survived preconditioning while adjacent bonds did not.

VII. OTHER CONSIDERATIONS

7.1 Device Rework

The ten test devices that had failed during prelidding burn-in were reworked. All of these devices were delidded using a grind-off technique. Nine of these devices had broken or melted bond wires which were replaced. The tenth device had a defective chip component which was replaced. Table 13 shows the failure percentage of reworked devices compared with that of all other (unreworked) devices. The substantial difference in failure percentage is not understood. The rework that was done was relatively simple and should not have affected failure percentage as much as it apparently did. Unfortunately, without conducting further experimentation, nothing more can be said about this.

TABLE 13

FAILURE PERCENTAGES OF REWORKED VERSUS UNREWORKED TEST DEVICES

Test Device Category	Electrical Test Point After	Number of Devices	Number of Failures	Failure Percentage	Type of Failure
Reworked	Precon-ditioning	10	2	20.0	Functional
	Sealed Lid Burn-in	8	1	12.5	Functional
	Life Testing	6	2	33.3	Parametric
	Accelerated Testing	1	1	100.0	Parametric
Unreworked	Precon-ditioning	94	10	9.5[a)]	Functional(9) Catastrophic(1)
	Sealed Lid Burn-in	84	10	1.2[b)]	Handling(11) Functional(1)

TABLE 13 (Cont.)

Test Device Category	Electrical Test Point After	Number of Devices	Number of Failures	Failure Percentage	Type of Failures
Unreworked (Cont.)	Life Testing	36	5	13.8	Parametric(4) Functional(1)
	Accelerated Testing	36	24	66.7	Parametric

a) This percentage reflects the nine functional failures only.

b) This percentage reflects the one functional failure only.

7.2 Nonhermetic Devices

During the experiment, 11 devices (seven control and four test) were found to be leakers. Three of these devices leaked at the seal while the other eight devices were pin leakers as shown in Table 14. The three devices that leaked at the seal were repaired by seam welding again. Since this rework did not involve removal of the package lids, it was decided to group these devices with the other nonhermetic devices rather than with the reworked devices discussed above. Two of the three resealed devices, both of them test devices, successfully passed 1,000 hours of life testing without functional or parametric electrical failure. The third device, a control device, failed at preconditioning and was found to have a broken aluminum bond wire. Three of the eight pin leakers passed 1,000 hours of life testing. The remaining five underwent 200 hours of accelerated testing. Two of these passed and three were parametric failures (one test and two control devices). It is concluded from this data that neither the resealing of the lids on four devices, nor the presence of pin leaks in eight devices, led to anomalous electrical behavior. Of the five devices that underwent 200 hours of accelerated testing, three (or 60%) exhibited

TABLE 14

PERFORMANCE OF NONHERMETIC DEVICES

Device Number	Type of Leak	Repaired? Yes	Repaired? No	Electrical Test Result After Preconditioning	Sealed Lid Burn-In	Life Testing	Accelerated Testing	Type of Failure
T121-05	Seal	X		Pass	Pass	Pass	N. T.	-
T321-05	Seal	X		Pass	Pass	Pass	N. T.	-
C021-04	Seal	X		Fail	N. T. [b]	N. T.	N. T.	Functional
T112-04	Pin		X	Pass	Pass	N. T.	Pass	-
T212-13	Pin		X	Pass	Pass	N. T.	Fail	Parametric
4[a]	Pin		X	Pass	Pass	Pass	N. T.	-
5[a]	Pin		X	Pass	Pass	N. T.	Fail	Parametric
41[a]	Pin		X	Pass	Pass	N. T.	Pass	-
84[a]	Pin		X	Pass	Pass	Pass	N. T.	-
88[a]	Pin		X	Pass	Pass	Pass	N. T.	-
149[a]	Pin		X	Pass	Pass	N. T.	Fail	Parametric

a) New control devices

b) N. T. = not tested

parametric failures. This failure percentage is consistent with that found in the experiment. These three devices were delidded using a grind-off technique and were examined for corrosion or other electro-chemical phenomena, caused by possible moisture penetration into the non-hermetic package, which could lead to device electrical failure. No corrosion, or other electro-chemical phenomena, was observed.

7.3 Failure Analysis

All of the functional failures that occurred during prelidding burn-in and sealed lid burn-in were visually examined and electrically probed from pin-to-pin in an attempt to identify failure location. Macrodata 501 test data was utilized for this effort. No failure analysis per se occurred on these devices; however, devices that exhibited parametric failure as a result of life testing were candidates for failure analysis. Six devices were selected as shown in Table 15. Three of these devices had undergone 1,000 hours of life testing and exhibited parametric shift. The fourth device, serial number 146, failed functionally after 240 hours of sealed lid burn-in. The fifth device, T211-13, failed functionally after 500 hours of life testing and the sixth device, C021-10, was an original control device that was catastrophically damaged. The results of these failure analyses are discussed in Appendix E, which contains the failure analysis report that was generated for these devices. The analyses revealed that two chips were overwhelmingly responsible for the functional and parametric failures that were examined. These chips were the CMOS CD4007 digital IC and the LSTTL 54LS112 digital IC.

TABLE 15

SUMMARY OF FAILURE ANALYSIS RESULTS

Device Number	Failed After	Type of Failure	Failure Analysis Results
T111-07	1000 Hours of Life Testing	Parametric	Degraded Output Section of Device IC4 (CMOS Digital IC)
T121-05	1000 Hours of Life Testing	Parametric	Degraded Input Gate Oxide of Device I2 (CMOS Digital IC)

TABLE 15 (Cont.)

Device Number	Failed After	Type of Failure	Failure Analysis Results
T421-12	1000 Hours of Life Testing	Parametric	Latched Outputs of Device FF3, 4 (LSTTL Digital IC)
146[a)]	240 Hours of Sealed Lid Burn-in	Functional	Degraded Input Gate Oxide of Device I2 (CMOS Digital IC)
T211-13	500 Hours of Life Testing	Functional	Degradation of Device IC4 (CMOS Digital IC)
C021-10	240 Hours of Sealed Lid Burn-in	Catastrophic	Overstressing at Pin 2

a) New control device

7.4 Leak Testing

The test plan specified that fine leak testing be performed after helium pressurization of the devices at 30 psig for four hours. Raytheon, Quincy reported that this pressure level had caused seal damage to devices packaged in similar welded, plug-in type packages on another program. To assure that the package seals of the devices used in this experiment were not impaired, it was decided to helium pressurize at 10 psig for eight hours minimum prior to fine leak testing. This pressurization condition was reported by Raytheon, Quincy to be equal to 30 psig for four hours. Gross leak testing was performed after fine leak testing. Ten psig pressurization was applied for 16 hours minimum to devices immersed in FC78 detector fluid. It was further decided that, at the end of the experiment, a group of devices that had seen 1,500 hours of life testing, would undergo fine leak testing per Method 1014.2, Condition A1 of MIL-STD-883B. This specified that 30 psig of helium pressurization be applied for four hours (+0.4, -0). It was then decided that these same 15 devices would undergo gross leak testing per Method 1014.2, Condition C of MIL-STD-883B. Thirty psig of pressurization was applied for 10 hours minimum. This fine and gross

leak testing was performed on 15 test devices that were first determined to be hermetic by leak testing performed as in the experiment. After exposure of these hermetic devices to 30 psig of helium for four hours, fine leak testing was performed. All devices passed. After pressurization had been completed, gross leak testing was performed. Again, all devices passed. It is concluded from this that these packages can be exposed to 30 psig pressurization without occurrance of damage to the seal and that use of 10 psig pressurization during the experiment was a needless precaution.

7.5 Bond Strength Testing

Destructive wire bond strength testing was performed on 60 gold wires and 12 aluminum wires in each of four dummy devices both before and after prelidding burn-in at 125°C in dry nitrogen and air. Virtually no change was noted in the strength of the gold wire which averaged about 7.5 grams. Not unexpectedly, the aluminum wires lost an average of 37.7% of their strength after 48 hours of prelidding burn-in in nitrogen and an average 32.9% of their strength after 48 hours of prelidding burn-in in air shown in Table 16. It was decided to perform additional bond strength testing on gold and aluminum wires of two devices that had undergone 168 hours of sealed lid burn-in at 125°C and two devices that had undergone 1,500 hours of life testing at 125°C. Again, no loss in strength in the gold wire occurred. The aluminum wire showed further strength loss. After 168 hours of sealed lid burn-in, the aluminum wires lost an average of 41.4% of their strength and an average of 43.7% of their strength after 1,500 hours of life testing. MIL-STD-883B, Method 2011.2, required a minimum pre-seal strength of bonds made with one mil diameter aluminum wires of 2.5 grams. After seal and any other processing or screening, a minimum bond strength of 1.5 grams is required. This represents a 40% loss of strength. Although the bond wires tested in this experiment lost slightly more than 40% of their strength after sealed lid burn-in and life testing, their actual average bond strengths were 4.42 and 4.25 grams respectively. This is well above the MIL-STD-883B minimum requirement.

TABLE 16

ALUMINUM WIRE BOND STRENGTH TESTING RESULTS

Test Point	Average Bond Strength (g)	Average Reduction in Strength (%)
Initial	7.54	-
After 48 hrs of Prelidding Burn-in in N_2	4.70	37.7
After 48 hrs of Prelidding Burn-in air	5.06	32.9
After 48 hrs of Prelidding Burn-in	4.42	41.4
After 1,500 hrs of Life Testing	4.25	43.7

7.6 Handling Related Device Failures

During the experiment, a total of 15 handling related device failures occurred. Three of these occurred during prelidding burn-in on, of course, test devices. Visual examination of these unsealed devices, coupled with electrical test data, revealed the cause of the failures to be broken or deformed wire bonds which subsequently shorted. In each instance, the bonds along one edge of the device, in a regular straight line pattern, were damaged. It was concluded that the package lid slipped into the package causing the observed damage. The unsealed lids were being used to cover and protect the devices and were removed only before insertion of the devices into the sockets for prelidding burn-in. After prelidding burn-in, devices were removed from the sockets and the lids were replaced, using ordinary rubber bands to attach the lids. Although only three devices out of 104 were damaged in this manner, this was three times the number of devices identified as a functional failure as a result of prelidding burn-in. Since the three damaged devices were not lidded, and since no catastrophic electrical or mechanical damage had occurred, rework could be performed. Improved handling techniques, however, are needed to prevent negation of

the beneficial aspects of prelidding burn-in by handling related damage. Use of a snap-on cover, made from metal foil or a semi-rigid plastic with a static sensitive coating, would provide more positive protection for the unsealed devices. Such covers would be removed only after the devices are mounted in burn-in sockets. After prelidding burn-in, covers would be replaced after cool down, prior to the removal of devices from the sockets.

The other 12 handling related failures occurred on sealed devices (11 test and 1 control) during sealed lid burn-in. All of these devices were delidded. Visual examination and pin-to-pin probing, coupled with Macrodata 501 electrical test data, led to the conclusion that the devices had been incorrectly inserted into sockets. It should be remembered that devices were exposed to much more handling during the conduct of the sealed lid burn-in portion of the experiment than would occur during normal burn-in. In some instances, as many as six insertion/removal cycles occurred compared to one insertion/removal cycle during normal burn-in. As the amount of handling increases, the number of handling related defects will, and did, increase. During sealed lid burn-in, handling related failures occurred after 48 hours (three test devices and one control device), after 96 hours (three test devices), and after 168 hours (five test devices). The configuration of the device package, and that of the burn-in sockets, led to the damage that occurred. The device packages contained 30 pins distributed ten to a side on three sides, whereas, the burn-in sockets contained 40 pins distributed ten to a side on four sides. This meant that the devices could be inserted in four orientations. The marking on device lids also served as a guide for insertion orientation; however, this in itself was evidently not sufficient. In this experiment, use of burn-in sockets containing 30 pins distributed ten to a side on three sides would have prevented improper insertion from occurring.

7.7 Gas Analysis

Four sealed devices, consisting of two dummy devices and two test devices that had successfully passed 1500 hours of life testing, were sent to RADC for mass spectrometric gas analysis per Method 1018 of MIL-STD-883B. Both of the dummy devices, which had not undergone any

type of burn-in testing and which represented the as-sealed condition, had water vapor contents less than the 6000 ppm maximum specified by MIL-STD-883B. Both of the test devices, however, had water vapor contents in excess of 6000 ppm as well as substantial amounts of other gases, some of which also had been found in the dummy devices but only in trace amounts. It is suspected that these other gases, which included methane and carbon dioxide, originated from the epoxy adhesives used to bond the chip components to the substrate and the substrate to the package. Both of the test devices were delidded using a grind-off technique and were examined. No evidence of corrosion, or other moisture-related electro-chemical phenomena, was observed.

VIII. CONCLUSIONS

As a result of the analysis performed on the test data generated by this experiment, the following conclusions can be drawn:

1) Is prelidding burn-in effective? Prelidding burn-in is envisioned as a means to identify and correct early device failures prior to sealing. This would minimize the amount of devices that require repair after sealing because of failures that occur during sealed lid burn-in. It was found that devices that had undergone pre-lidding burn-in failed at a lower rate during sealed lid burn-in than devices that were not pre-lid burned-in (2.2% versus 5.7%). Based on this, it is concluded that prelidding burn-in is effective.

The sealed lid burn-in failure rate that occurred in this experiment on the hybrid circuit test vehicle, which contains 18 active chip components, compared well with recent Raytheon, Quincy production (sealed lid) burn-in data. For one device that contained 11 active components, burn-in failure rate was 4.0%. This device was burned-in at 85 °C for 168 hr. Another simpler device, that contained only one bipolar transistor, had a burn-in failure rate of only 2.0% when burned-in at 125 °C for 168 hr. Another more complex device, which contained 20 digital 54L IC chips, had a burn-in failure rate of about 12.5% when burned-in at 125 °C for 168 hr.

The use of prelidding burn-in should be optional. Its use should be a function of the complexity of the hybrid device in question coupled with, if available, actual sealed lid burn-in failure rates. Single packaged components or hybrid devices containing only a few active chip components would not make good candidates for prelidding burn-in unless sealed lid burn-in failure percentages are high. As hybrid device complexity increases, and the number of active chip components increases,

the potential for defects likewise increases as well as the cost of the device. In devices such as these, the use of prelidding burn-in is indeed desirable.

2) Is prelidding burn-in non-destructive? After 1,000 hr of life testing at 125°C, less parametric failures occurred on devices that had undergone prelidding burn-in than occurred on control devices (14.3% versus 20%). After 200 hr of accelerated testing at 150°C, failure percentage of devices that had undergone prelidding burn-in was approximately the same as for control devices (67.6% versus 60%). Based on this, prelidding burn-in is considered to be nondestructive.

3) What is the optimum environment for prelidding burn-in? The test devices that underwent prelidding burn-in at 125°C in air had a slightly higher average failure percentage after 1,000 hr of life testing than did test devices that underwent prelidding burn-in at 125°C in dry nitrogen (16.7% versus 13.8%). For this reason, a dry nitrogen environment is preferred.

None of the test device groups that underwent prelidding burn-in with the oven fan on, or in a Class 10,000 maximum environment, had life test failure percentages greater than the control devices. Based on this, a Class 10,000 maximum environment is allowable.

4) What is the optimum burn-in time duration and temperature before and after lidding? Very few prelidding or sealed lid burn-in related failures occurred in this experiment. The one prelidding burn-in related failure that did occur was at 25°C after 24 hr. Based on this data it could be concluded that prelidding burn-in should be performed at 25°C for 24 hr; however, it is felt that this would not sufficiently stress the devices. Since life test data revealed that no failure rate increase occurred on devices that underwent prelidding burn-in at 125°C for 48 hr, it is concluded that a prelidding burn-in temperature of 125°C should be used. Sinc· -elidding burn-in

is intended to identify defects so that repair can be performed prior to sealing, it is felt that a period of high stress, unlidded burn-in, longer than 24 hr would be desirable. Based on this, it is concluded that prelidding burn-in should be performed for 48 hr.

Experimental data suggests that sealed lid burn-in should be performed at 125 °C for 168 hr; however, it is felt that the less stringent MIL-STD-883B, Method 5008 requirements represent an acceptable risk and should continue to be invoked. These requirements permit division of the total minimum burn-in time of 160 hr at 125 °C between prelidding and sealed lid burn-in provided that the total burn-in time equals or exceeds the specified 160 hr burn-in time and that the sealed lid burn-in time equals or exceeds 96 hr.

5) What are the temperature/time tradeoffs? For prelidding burn-in, use of 125 °C temperature for 48 hr maximizes the chance for failure of a defective or marginal device. If a lower test temperature than 125 °C is used, a corresponding increase in test time is necessary. Reduction in test time below 48 hr can only be done if historical electrical test data, taken after the proposed test time, compares favorably in terms of failure percentage with test data taken after 48 hr. Modification of test temperature or time can be done only with the approval of the procuring activity.

6) What is the effect of rework? A comparison of reworked device failure percentages with unreworked device failure percentages indicated that rework had a deleterious effect; however, it is not understood why. More study is needed before satisfactory answers can be formulated.

7) What is the proper way to handle unsealed devices? Unsealed devices must be covered at all times for protection against handling induced defects. Three of the ten devices that failed during prelidding burn-in were as a result of poor handling. In this experiment, the actual package lids were used to protect the device. A more suitable procedure would be to use covers, made from metal foil or semi-rigid plastic with a static sensitive coating, that would be removed only after all devices are in place in the burn-in racks, and then replaced after burn-in and cool-down prior to removal of devices from the burn-in racks.

IX. RECOMMENDATIONS

It is recommended that a MIL-STD-883 method for prelidding burn-in of hybrid circuits be written. This recommendation is based on the favorable findings of this evaluation.

APPENDIX A

PHOTOMACROGRAPHS OF CHIP COMPONENTS INCORPORATED

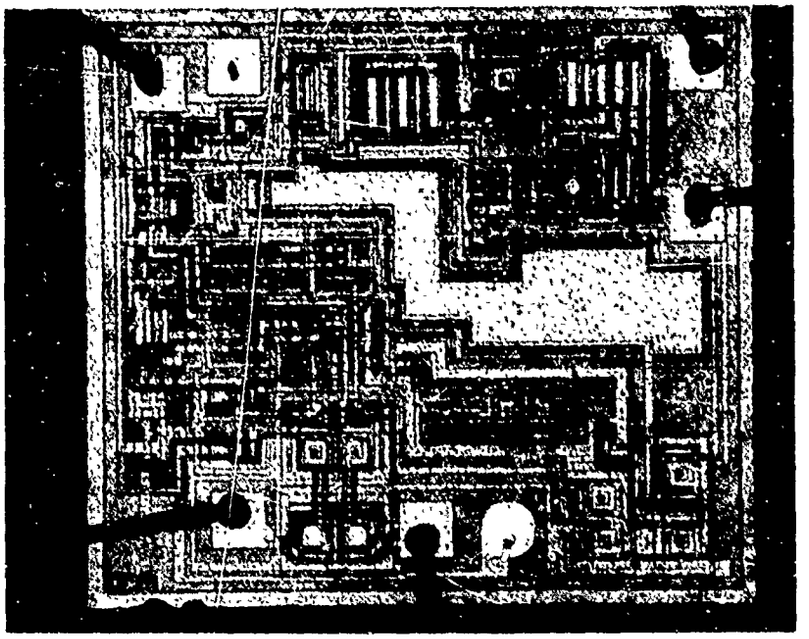


Figure A-1 - Linear IC, Bipolar, LM741, Component IC1, 60X Magnification

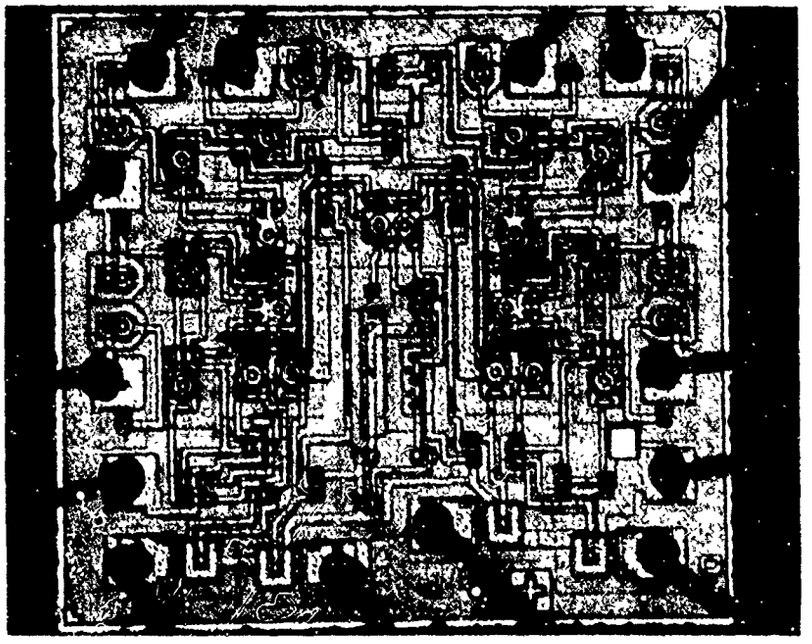


Figure A-2 - Linear IC, Bipolar, LM139, Component IC2, 3, 52X Magnification

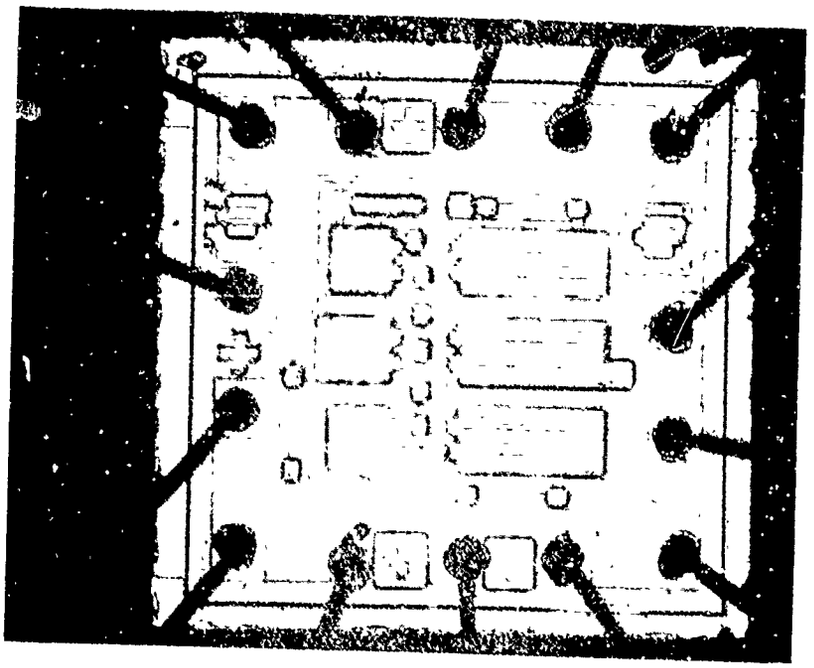


Figure A-3 - Digital IC, CMOS, CD 1007, Components 11, 2, 3 IC4, IC5, 56X Magnification

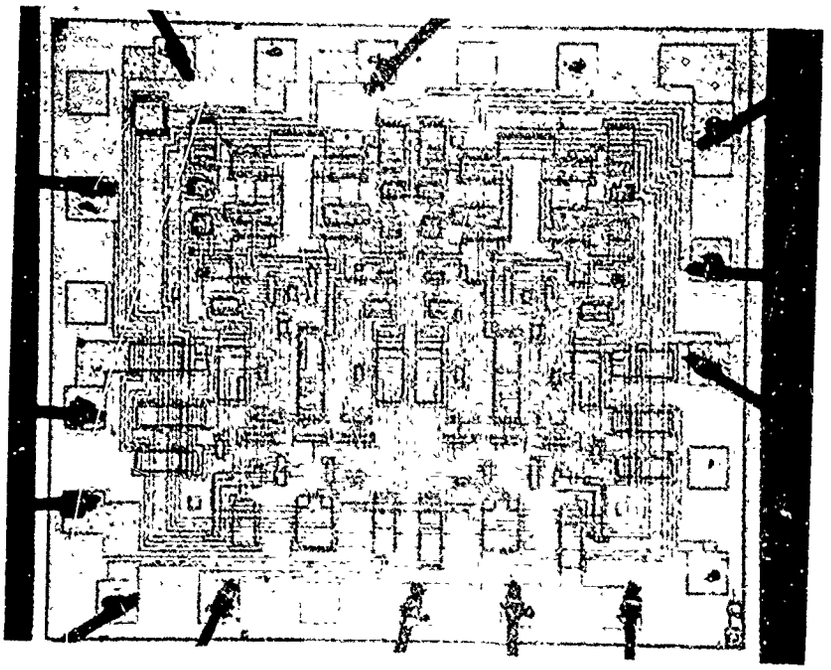


Figure A-4 - Digital IC, LSTTL, 9LS112, Components FF1, 2, FF3, 4, 58X Magnification

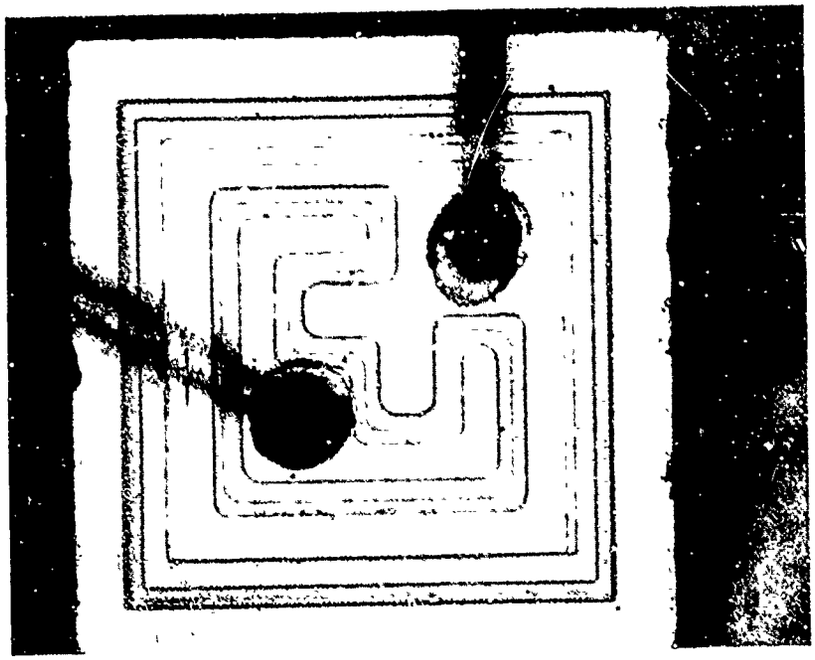


Figure A-5 - Transistor, Bipolar, 2N2222, Components Q1, Q2, 160X Magnification

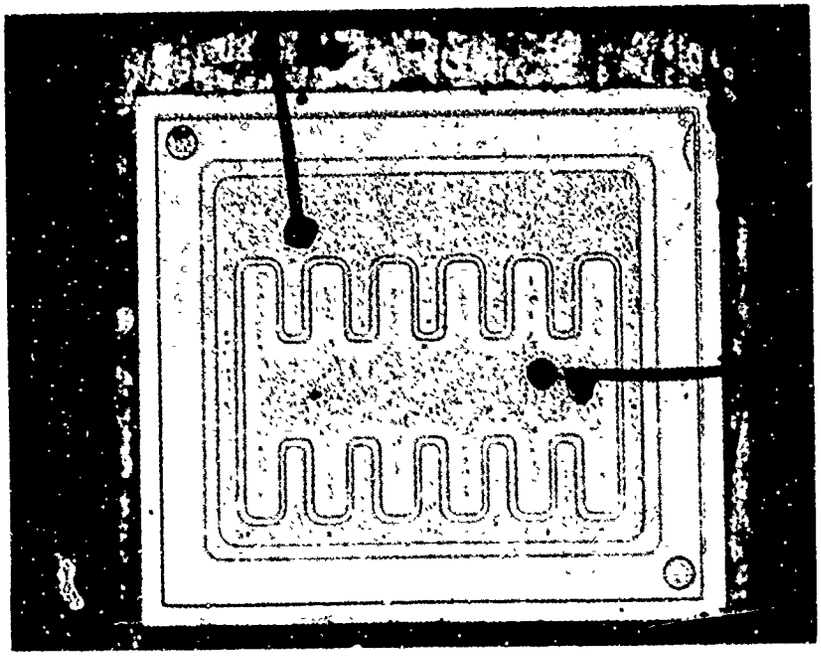


Figure A-6 - Transistor, Bipolar, 2N4237, Component Q3, 15X Magnification

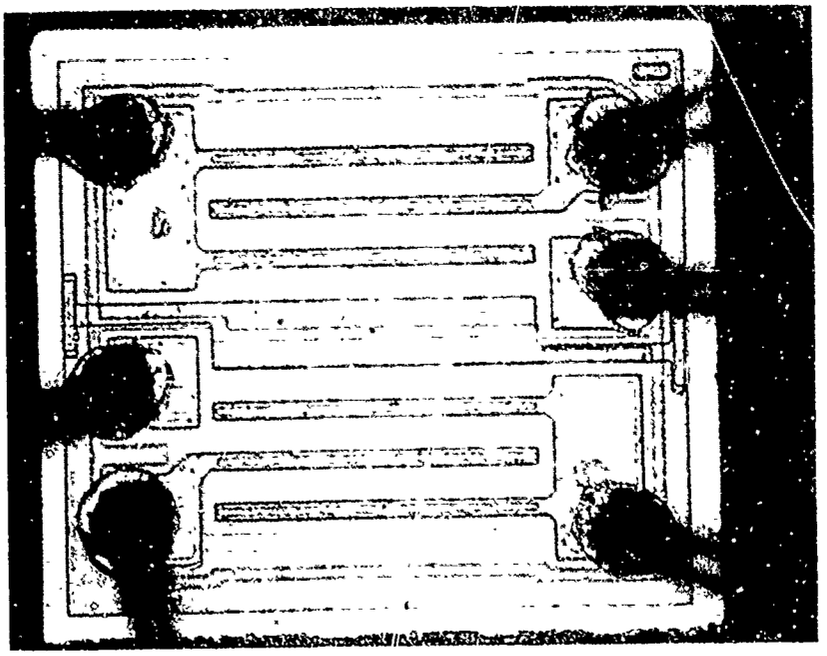


Figure A-7 - Transistor, FET, 2N3967, Component Q3, 4, 160X Magnification

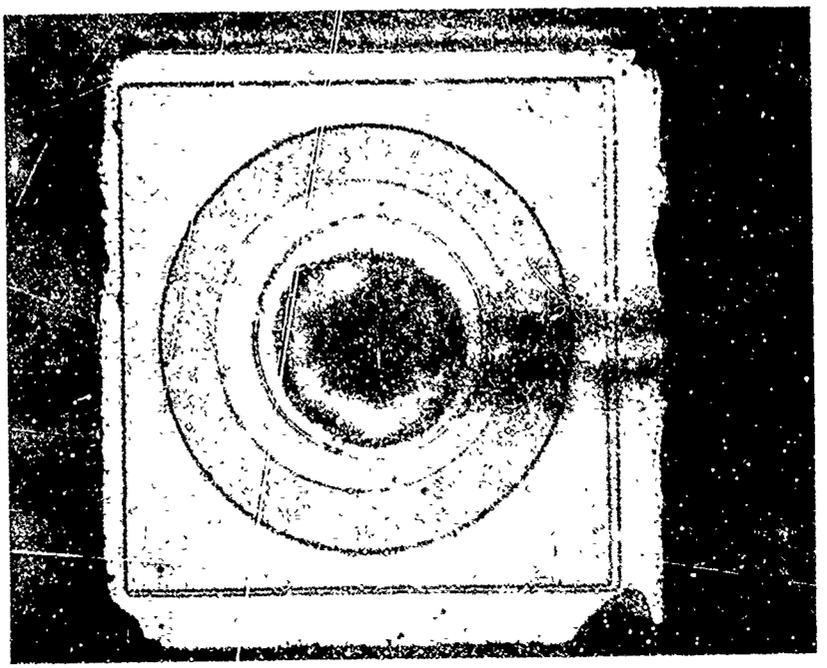


Figure A-8 - Diode, Diffused, IN3600, Components CR1, CR2, CR3, CR4, 200X Magnification

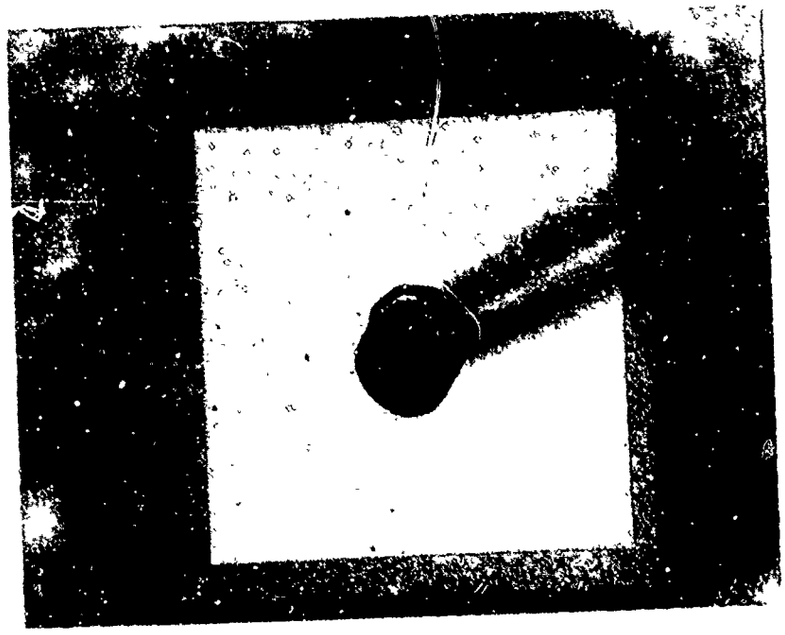


Figure A-9 - Diode, Schottky, HP5082-0087, Components CR5, CR6, 200X Magnification

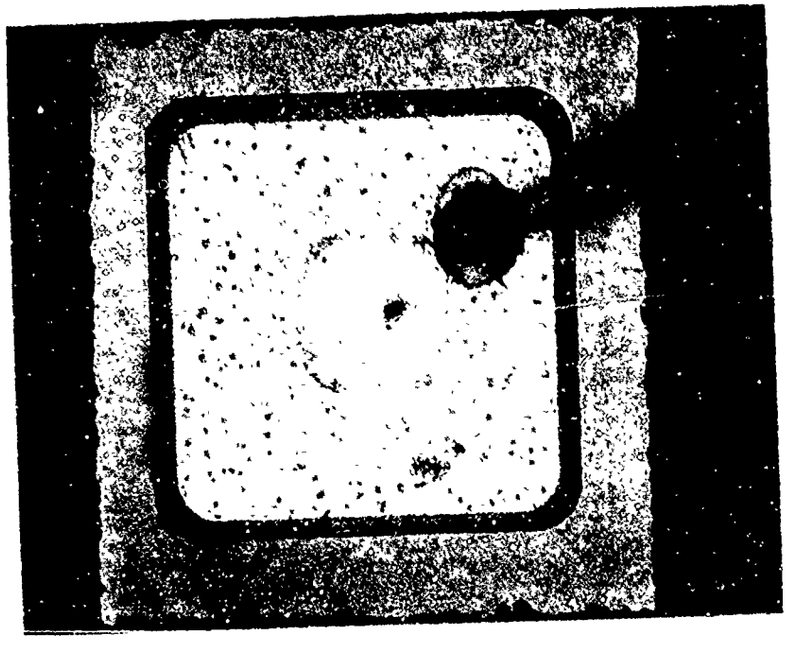


Figure A-10 - Diode, Zener, 1N5232, Component VR1, 160X Magnification

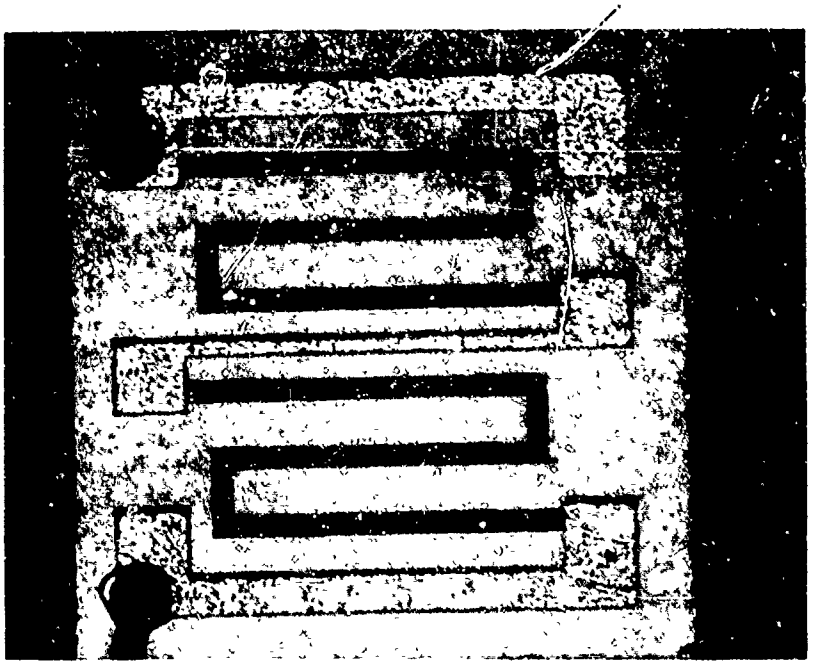


Figure A-11 - Resistor, Thin Film, 10kΩ, Components R6, R7, R12, 110X Magnification

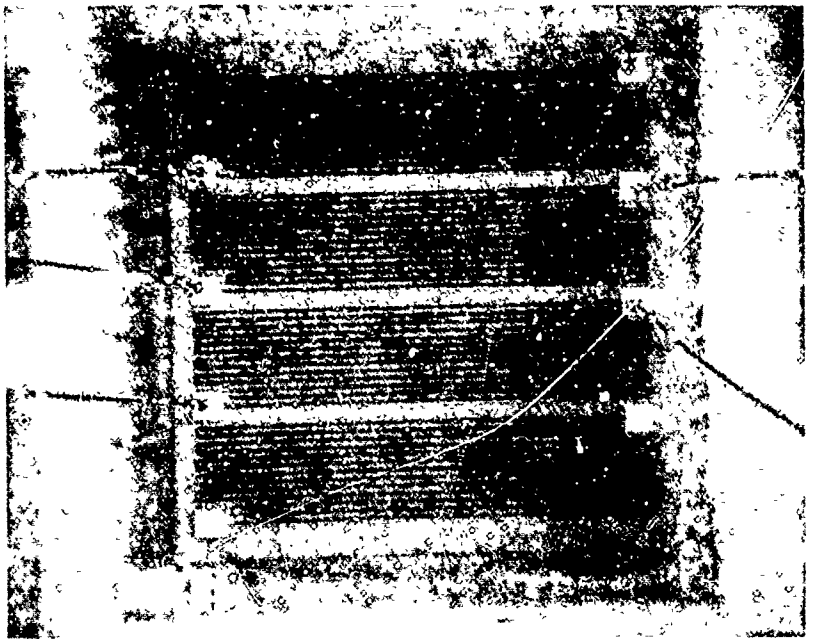


Figure A-12 - Resistor, Thin Film, 100 kΩ, Components R13, R15, R16, 28X Magnification

APPENDIX B
MACRODATA 501 ELECTRICAL TEST DETAILS

TABLE B1

MACRODATA 501 PARAMETRIC ELECTRICAL TEST DETAILS: +25°C

Test No.	Component Designation	Measured Pins +	Measured Pins -	Electrical Limits	Forced Quantity	Description[a)]
1	Q5	2	1	0.459 to 0.561V	100 μA	V_{be} of Q5
2	Q5	1	2	1.08 to 1.32V	100 μA	V_{eb} of Q5
3	VR1	2	12	0.935 to 1.14V	200 μA	V_z of VR1
4	VR1	12	2	0.594 to 0.726V	100 μA	V_{fz} of VR1
5	VR1	12	2	0.810 to 0.990V	500 μA	V_{fz} to VR1
6	VR1	12	2	1.22 to 1.49V	5 mA	V_{fz} of VR1
7	IC4	3	12	0 to 20 mV	sensed	V_{OL} of IC4
8	IC4	3	12	4.9 to 5.1V	sensed	V_{OH} of IC4
9	CR5	7	9	0.25 to 0.33V	100 μA	V_{FZ} of CR5
10	CR5	7	9	0.400 to 0.550V	5 mA	V_{FZ} of CR5
11	CR6	7	8	0.25 to 0.33V	100 μA	V_{FZ} of CR5
12	CR6	7	8	0.400 to 0.500V	5 mA	V_{FZ} of CR6
13	CR5	9	7	21 to 28V	500 μA	V_Z of CR5
14	IC6	8	7	21 to 28V	500 μA	V_Z of CR6
15	IC5	9	12	0 to 15 mV	sensed	V_{OL} of IC5
16	IC5	9	12	4.9 to 5.1V	sensed	V_{OH} of IC5
17	CR2	13	10	0.423 to 0.517V	100 μA	V_f of CR2
18	CR2	13	10	0.603 to 0.737	5 mA	V_f of CR2
19	CR1	13	15	0.423 to 0.517V	100 μA	V_f of CR1
20	CR1	13	15	0.603 to 0.737V	5 mA	V_f of CR1
21	CR2	10	13	7.2V to 8.8V	500 μA	BV of CR2
22	CR1	15	13	5.7V to 7.7V	500 μA	BV of CR1
23	CR3	19	16	0.423 to 0.517V	100 μA	V_f of CR3
24	CR3	19	16	0.603 to 0.737V	5 mA	V_f of CR3
25	CR4	19	17	0.423 to 0.517V	100 μA	V_f of CR4
26	CR4	19	17	0.603 to 0.737V	5 mA	V_f of CR4
27	CR3	16	19	0.1 μA to -20 μA	25V	I_r of CR3
28	CR4	17	19	0.1 μA to -20 μA	25V	I_r of C_{r4}

TABLE B1 (Cont.)

Test No.	Component Designation	Measured Pins +	Measured Pins -	Electrical Limits	Forced Quantity	Description[a]
30	FF4	15	12	50 to 400 mV	sensed	V_{OL} of T^2L FF
30	FF4	16	12	50 to 400 mV	sensed	V_{OL} of T^2L FF
31	FF4	15	12	15 to 100 mA	OV	I_{OS} of FF4
32	FF4	16	12	15 to 100 mA	OV	I_{OS} of FF4
33	FF4	15	12	2.5 to 4.6V	sensed	V_{OH} of FF4
34	FF4	16	12	2.5 to 4.6V	sensed	V_{OH} of FF4
35	All FF	21	12	500 to 3,200 mA	OV	I_{IL} of All FF
36	All FF	21	12	15 to 26V	100 μA	V_{BI} of All FF
37	All FF	21	21	-0.75 to -0.65V	100 mA	V_{FIN} of All FF
38	FF2,3	22	12	-300 to +300 μA	5V	I_{IH} and I_{OLK} of FF2,3
39	FF2	22	12	50 to 400 mV	sensed	V_{OL} of FF2
40	FF2	22	12	-500 to +300 μA	5V	I_{IH} and I_{OLK} of FF2
41	FF1	29	12	50 to 400 mV	sensed	V_{OL} of FF1
42	All FF	20	12	200 to 700 μA	1V	I_{CC} of All FF
43	IC2	23	12	80 to 160 mV	40 μA	V_{OL} of IC2
44	IC3	24	12	50 to 300 mV	4 μA	V_{OL} of IC3
50	Q3	30	12	400 to 700 mV	50 μA	V_{FG-DS} of Q3
51	R20	10	12	-0.24 to -0.19V	40 μA	5K Resistor
52	R19	17	12	-0.24 to -0.19V	40 μA	5K Resistor
53	R18	18	19	-0.24 to -0.19V	40 μA	5K Resistor
54	R17	14	13	-0.24 to -0.19V	40 μA	5K Resistor
55	R15	1	7	-0.50 to -0.34	4 μA	100K Resistor
56	R16	8	12	-0.50 to -0.34	4 μA	100K Resistor
57	R13	24	1	-0.50 to -0.34	4 μA	100K Resistor
58	R12	23	1	-34 to -50 mV	4 μA	10K Resistor
59	R10, R11	12	25	-2.2 to -1.8V	25 mA	Two 1K Resistor
60	R9	28	26	-0.22 to -0.18V	7 μA	30K Resistor
61	R14	20	14	-1.1 to -0.9V	85 μA	5K Resistor

a) Results were altered by paralleled circuitry.

TABLE B2

MACRODATA 501 FUNCTIONAL ELECTRICAL TEST DETAILS: +25°C

Test No.	Component Designation	Measured Pin	Electrical Limits	Description[a]
1	IC4	3	4.8 to 5.2V	Level Check
2	IC4	3	10 to 40 mV	Level Check
3	CR5	7	200 to 400 mV	Level Check
4	CR5	7	2.3 to 2.9V	Level Check
5	CR6	8	2 to 2.6V	Level Check
6	CR6	8	10 to 200 mV	Level Check
7	IC5	9	10 to 200 mv	Level Check
8	IC5	9	4.8 to 5.2V	Level Check
9	CR2	10	1.65 to 2.75V	Level Check
10	CR2	10	200 to 400 mV	Level Check
11	CR1	13	500 to 800 mV	Level Check
12	CR1	13	2.2 to 3.3V	Level Check
13	FF4	15	2.5 to 4.6V	Level Check
14	FF4	15	50 to 400 mV	Level Check
15	FF4	16	2.5 to 4.6V	Level Check
16	FF4	16	50 to 400 mV	Level Check
17	CR4	17	200 to 400 mV	Level Check
18	CR3	19	1.65 to 2.75V	Level Check
19	CR3	19	2.2 to 3.3V	Level Check
20	CR3	19	500 to 800 mV	Level Check
21	FF2	22	2.5 to 4.6V	Level Check
22	FF2	22	50 to 400 mV	Level Check
23	FF1	29	50 to 400 mV	Level Check
24	FF1	29	2.5 to 4.6 mV	Level Check
25	IC2	23	4 to 5.1V	Level Check
26	IC2	23	40 to 140 mV	Level Check
27	IC3	24	0 to 0.1V	Level Check
28	IC3	24	4 to 5.1V	Level Check
31	Q3	30	55 to 85 μsec	Period Measurement
32	IC1	26	2 to 4.4V	Level Check

TABLE B2 (Cont.)

Test No.	Component Desigation	Measured Pin	Electrical Limits	Description[a)]
33	IC1	28	2 to 4V	Level Check
34	Q3	30	2 to 4V	Level Check
35	IC1	26	-2V to 0V	Level Check
36	IC1	28	-1V to 0V	Level Check
37	Q3	30	-4V to -2V	Level Check
38	IC4	3	55 to 85 μsec	Period Measurement
39	CR5	7	55 to 85 μsec	Period Measurement
40	CR6	8	55 to 85 μsec	Period Measurement
41	IC5	9	55 to 85 μsec	Period Measurement
42	CR2	10	880 to 1,360 μsec	Period Measurement
43	CR1	13	880 to 1,360 μsec	Period Measurement
44	FF4	15	880 to 1,360 μsec	Period Measurement
45	FF4	16	880 to 1,360 μsec	Period Measurement
46	CR4	17	880 to 1,360 μsec	Period Measurement
47	CR3	19	880 to 1,360 μsec	Period Measurement
48	FF2	22	220 to 340 μsec	Period Measurement
49	IC2	23	55 to 85 μsec	Period Measurement
50	IC3	24	55 to 85 μsec	Period Measurement
	FF1	29	110 to 170 μsec	Period Measurement

a) The test vehicle built-in oscillator was allowed to function. Resulting voltage levels were sensed. Resulting frequencies were measured while the device was operating.

APPENDIX C
MACRODATA 501 COMPUTER PROGRAM

The Macrodata 501 Automatic Test System was used to test the hybrid circuit test vehicle. Testing was accomplished by using a main calling program for each of the three test temperatures. Figure C1 is a listing of the +25°C main calling program. This program: reserves data cells; connects, selects and sets up pins, modes and values for initial conditions; and then calls up the appropriate set of 20 major subroutines to accomplish all of the parametric and functional testing. Of these 20 major subroutires, 11 are listed in the main calling program and the other nine are called up by one of the listed 11. Figure C2 is a printout of one of these subroutines, number 35237, which sets up conditions and limits for parametric tests 35, 36 and 37.

Parametric testing was performed with the test vehicle built-in oscillator disabled. External clocking was provided by the test system to bring the pin under test to the proper state, whereupon, the electric value at the pin under test was measured and logged.

Functional testing was performed with the test vehicle built-in oscillator in operation. The test system then interrogated the pin under test to determine when the proper state was obtained and then sensed the voltage at that pin. This interrogation and sensing method was also used to measure the various frequencies generated by the hybrid circuit test vehicle. These values were measured and logged.

```
      OPEN = S6789
      LOEF = DA1
      LOEF = DA2
      LOEF = DA3
      LOEF = DA4
      LOEF = DA5
      LOEF = DA6
      LOEF = DA7
      LOEF = DA8
      LOEF = DA9
      LOEF = DA10
      LOEF = DA11
      LOEF = DA12
      LOEF = DA13
      LOEF = DA14
      LOEF = DA15
      LOEF = DA16
      LOEF = DA17
      LOEF = DA18
      LOEF = DA19
      LOEF = DA20
      LOEF = DA21
      LOEF = DA22
      LOEF = DA23
      LOEF = DA24
      LOEF = DA25
      LOEF = DA26
      LOEF = DA27
      LOEF = DA28
      LOEF = DA29
      LOEF = DA30
      LOEF = DA31
      LOEF = DA32
      LOEF = DA33
      LOEF = DA34
      LOEF = DA35
      LOEF = DA36
      LOEF = DA37
      LOEF = DA38
      LOEF = DA39
      LOEF = DA40
      LOEF = DA41
      LOEF = DA42
      LOEF = DA43
      LOEF = DA44
      LOEF = DA45
      LOEF = DA46
      LOEF = DA47
      LOEF = DA48
      LOEF = DA49
      LOEF = DA50
      LOEF = DA51
   10 SUNE = TPFHD,OLD,DISC1
      COCT = PEMO,DCUN,0-63
      COCT = REMA,OPEN,0-63
      COCT = REMA,NOSE,0-63
      COCT = REMA,NORE,0-63
      SECT = PHEL,RESE
      SECT = SEER,DRIVER
      SECT = FAIL,REC MX
      SECT = FAIL,REC MN
      SECT = FAIL,DRIVER V LIMIT
      SECT = FAIL,NOT DI LIMIT
      SECT = FAIL,POWER A LIMIT
      SECT = FAIL,NOT A NOT LIMIT
      SECT = REER,DEVICE
      SECT = TECO,SILE
      EQTE = TIDO,50
      EQTE = PORA,5
      EQTE = PORB,-5
      EQTE = PORC,12
      EQTE = DRVO,5.5
      EQTE = DRCU,100
      EQTE = FOCU,0
      EQTE = NSQ2, 1
      LOAD = EMGR
      LOAD = PPGR
      LOAD = CHGR
      SUNE = TPF01212,OLD,DISC1
      SUNE = TPF13221,OLD,DISC1
      SUNE = TPF22228,OLD,DISC1
      SUNE = TPF29234,OLD,DISC1
      SUNE = TPF35237,OLD,DISC1
      SUNE = TPF38239,OLD,DISC1
      SUNE = TPF40242,OLD,DISC1
      SUNE = TPF43250,OLD,DISC1
      READ = HEAS
      CORE = HEAS,04
      GO = 15
      LOG
   15 SUNE = TPF51262,OLD,DISC1
      READ = HEAS
      CORE = HEAS,04
      GO = 20
      LOG
   20 SUNE = TPF2345,OLD,DISC1
      READ = HEAS
      CORE = HEAS,04
      GO = 25
      LOG
   25 IF = FOCU,0
      GO = 30
      GO = 30
      LOAD = HAER,14
      GO = 10
   30 LOAD = HAER,10
      GO = 10
      END
      CLOSE = S6789
```

Figure C-1 - Main Calling Program

```
1           OPEN = S35237
2           SECT = EM.F-DI
3           COCT = PEMO.DCUN.0-63
4           SUNE = 90
5           SECT = SEER.OPEN
6           SECT = FAIL.NODV
7           COCT = REMA.SECE.21
8           COCT = REMA.PORA.20
9           COCT = PEMA.PORC.12
10          EQTE = MAVO.-1
11          EQTE = PORA.5
12          EQTE = PORC.0
13          EQTE = CUNN.500
14          EQTE = CUMX.3200
15          LOAD = APGR
16          LOAD = PPGP
17          LOAD = CHGP
18          SUNE = 110
19          EQTE = DA15.BRVO
20          SUNE = 90
21          SECT = SEER.DRIVER
22          SECT = FAIL.DRVL
23          COCT = PEMA.SECE.21
24          COCT = REMA.GRND.12
25          COCT = REMA.PORA.20
26          EQTE = PORA.5
27          EQTE = MAVO.1
28          EQTE = DRVO.28
29          EQTE = DRCU.100
30          EQTE = VOMN.15
31          EQTE = VOMX.3
32          LOAD = APGP
33          LOAD = PPGP
34          SUNE = 110
35          EQTE = DA36.BRVO
36          SUNE = 90
37          COCT = PEMA.SECE.21
38          COCT = PEMA.GRND.12
39          EQTE = DRVO.-5 5
40          EQTE = DRCU.10000
41          EQTE = VOMN.-75
42          EQTE = VOMX.-66
43          LOAD = APGR
44          SUNE = 110
45          EQTE = DA37.BRVO
46          RETURN
47          *  RETURN TO MAIN
48       90 COCT = REMA.OPEN.0-63
49          COCT = PEMA.NOSE.0-63
50          COCT = REMA.NORE.0-63
51          RETURN
52      100 EQTE = STVO.VOMN
53          END = 21
54          MULY = STVO.NSQ2
55          EQTE = VOMX.STVO
56          ADD = VOMX.VOMN
57          SUCT = VOMN.STVO
58          END = 22
59          RETURN
60      105 EQTE = STVO.CUNN
61          MULY = STVO.NSQ2
62          EQTE = CUMX.STVO
63          ADD = CUMX.CUMN
64          SUCT = CUMN.STVO
65          RETURN
66      110 END = 10
67          ADD = DA0.1
68          EQTE = FAFL.0
69          EQTE = DIBU.CLAR
70          LOAD = TECO
71      120 SESE = APST
72          COPE = APST.08
73          GO = 130
74          GO = 120
75      130 CURE = APST.80
76          GO = 140
77          EQTE = FAFL.1
78          EQTE = FOCU.1
79          EQTE = BUPO.4
80          EQTE = DIBU.'XX FAILED XX'
81      140 IF = DA62.0
82          GO = 160
83          GO = 160
84          IF = DA63.0
85          GO = 150
86          GO = 150
87          IF = FAFL.0
88          GO = 160
89          GO = 160
90      150 IF = MAVO.0
91          GO = 152
92          GO = 152
93          GO = 154
94      152 SUNE = TPFLPRT.OLD.DISC1
95          GO = 170
96      154 SUNE = TPFVPRT OLD.DISC1
97          GO = 170
98      160 IF = MAVO.0
99          GO = 165
100         GO = 165
101         READ = VOVA
102         EQTE = BRVO.VOVA
103         MULY = BRVO.1000
104         GO = 170
105     165 READ = AMVA
106         EQTE = BRVO.AMVA
107     170 RETURN
108         SUNE = TPF35237.NEW.DISC1
109         END
110         CLOSE = S35237
```

Figure C-2 - Example of a Called Subroutine

APPENDIX D
REPRESENTATIVE ELECTRICAL TEST RESULT HISTOGRAMS

Complete sets of histograms, similar to the set for test 7 in the body of the report, were generated for seven additional selected parametric tests as shown in Table D1. From these histograms, some were selected for inclusion in this Appendix. For test 14, which is a measure of the reverse leakage of the Schottky diodes, histograms, showing initial test data and post 1,000 hours life test data taken at -55, 25 and 125°C are included. For the other six parametric tests, histograms showing initial and post 1,000 hour life test data at 25°C only are included.

Examination of the histograms included in this Appendix revealed that, while some parametric shift did occur on some components, none can compare to the amount of shift that occurred on the CMOS ICs as shown in the test 7 histograms. It should be pointed out that shift was not restricted to test devices only; control devices also shifted. This demonstrated that parametric shift was not exclusively associated with devices that had undergone pre-lidding burn-in. The Schottky diodes, the diffused diodes, the LM139 comparators, and the JFET transistors were stable. Some shift occurred in the LSTTL ICs; however, only one device exceeded test limits after life testing. Less shift occured in thick film resistors after life testing than before. The thin film resistors in one device shifted beyond test limits after life testing.

TABLE D-1

DESCRIPTION OF REPRESENTATIVE HISTOGRAMS

Test Number	Component Tested	Value Measured
14	CR6, Schottky Diode	V_{ZR} @ 100 μA
28	CR4, Diffused Diode	I_R @ -25V
38	FF2, FF3, Digital IC, LSTTL, 54LS112	I_{IH}/I_{OLK} @ OV
47	IC2, IC3, Linear IC, Bipolar, LM139	V_{BE} @ I = 50 A
50	Q3, Transistor, FET,	V_{FG-DS} @ I = 50 μA
54	R17, Thick Film 5 KΩ Resistor	Ω @ I = 40 μA
57	R13, Thin Film 100 KΩ Resistor	Ω @ I = 4 μA

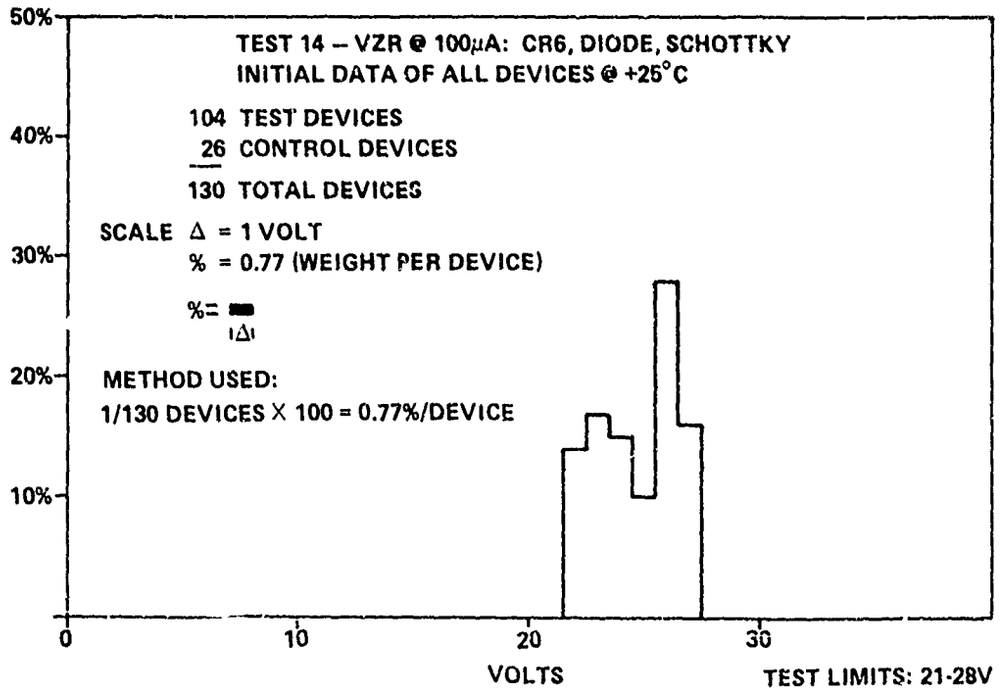


Figure D-1 - Test 14, Initial 25°C Data

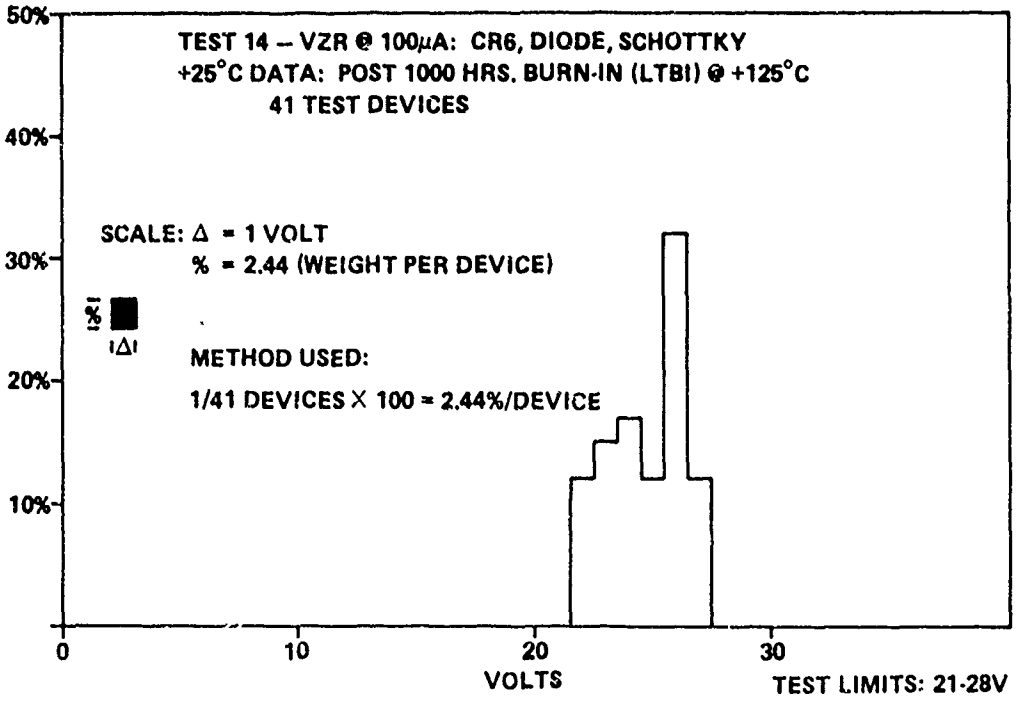


Figure D-2 - Test 14, Post 1000 Hours at 125°C Data (25°C)

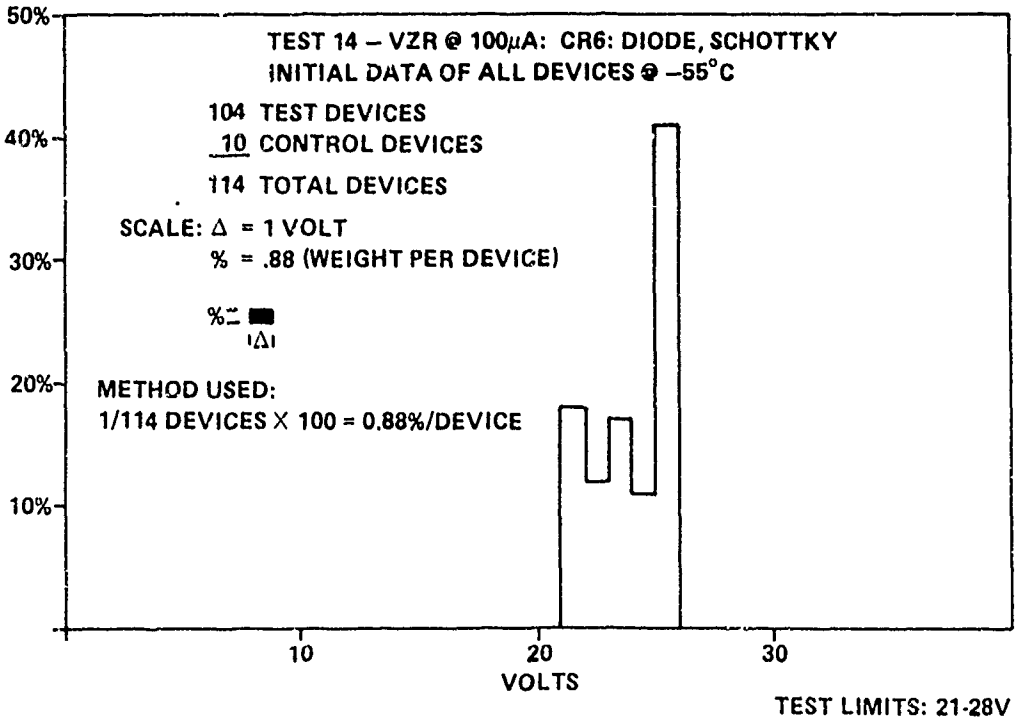


Figure D-3 - Test 14, Initial -55°C Data

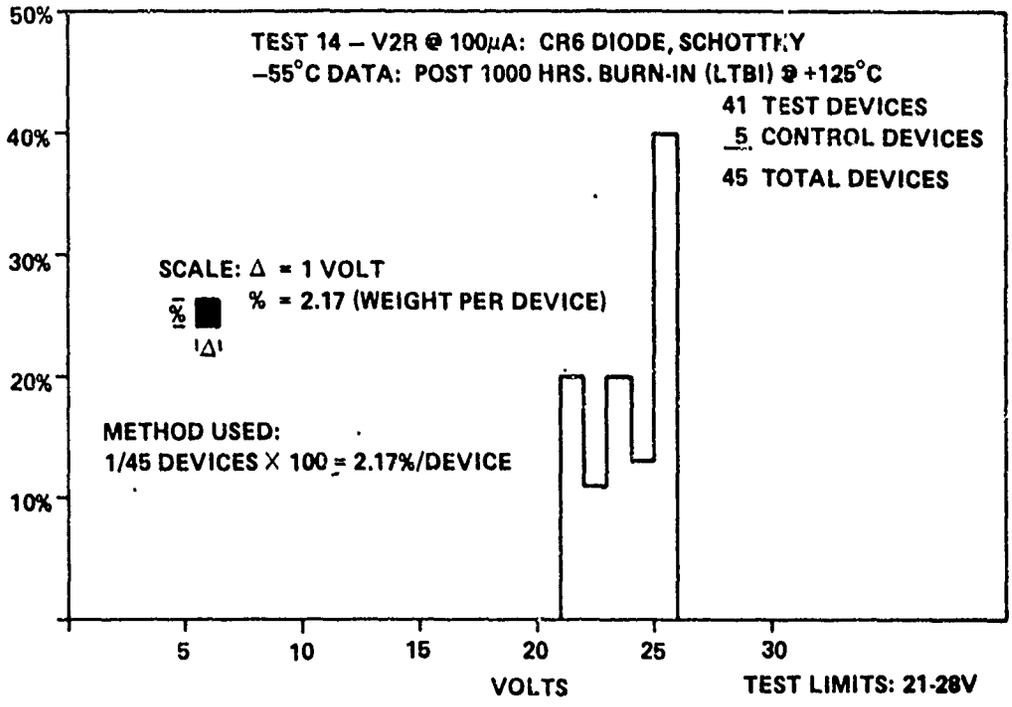


Figure D-4 - Test 14, Post 1000 Hours at 125°C Data (-55°C)

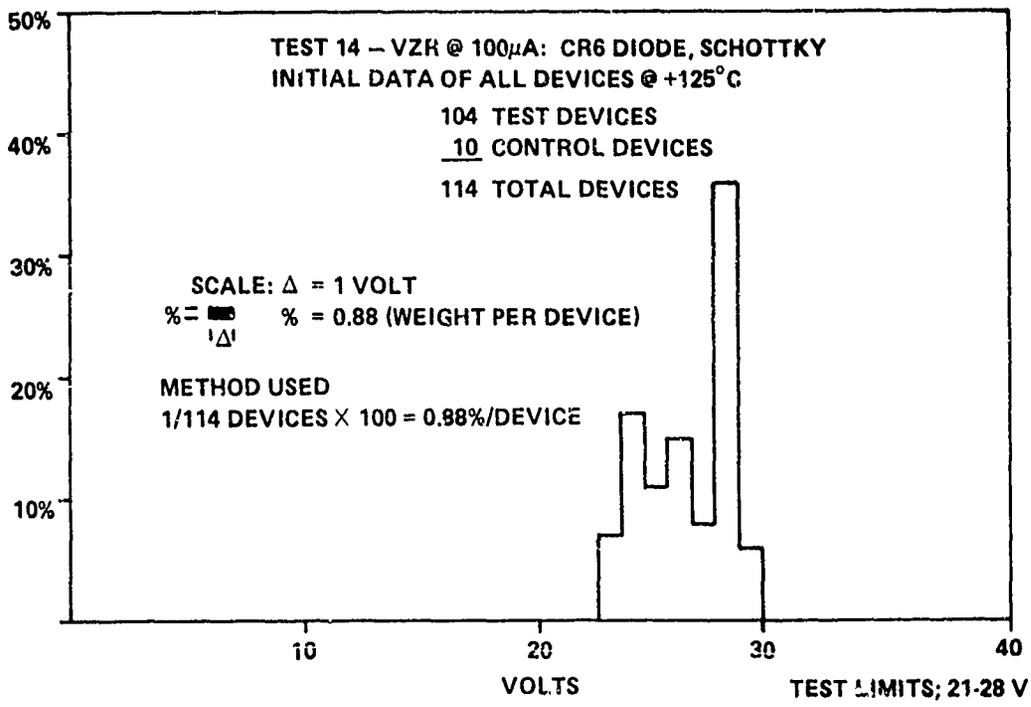


Figure D-5 - Test 14, Initial 125°C Data

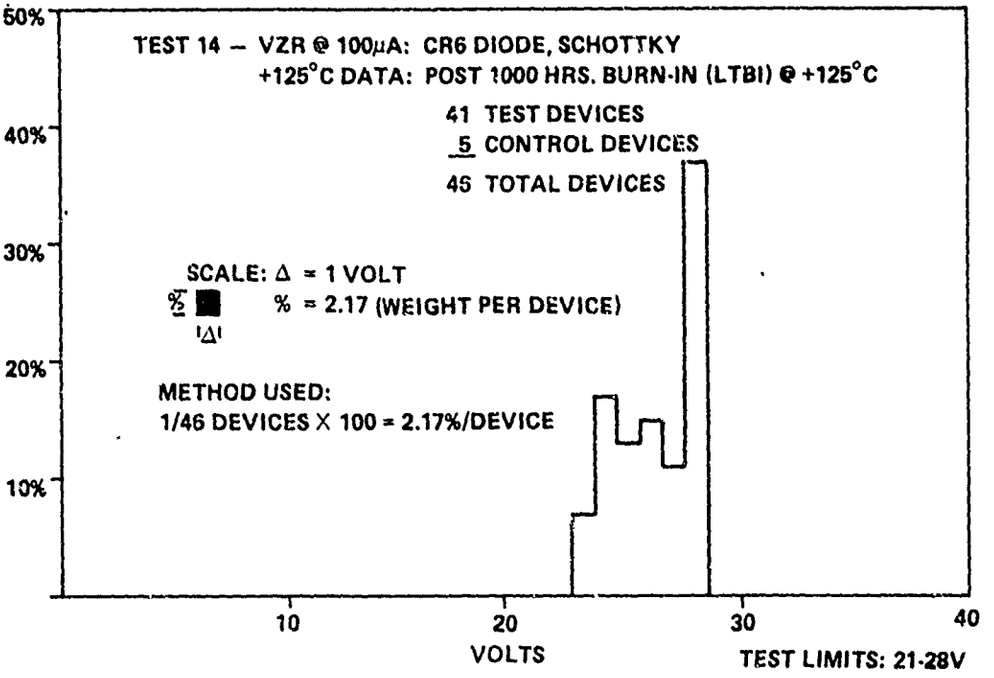


Figure D-6 - Test 14, Post 1000 Hours at 125°C Data (125°C)

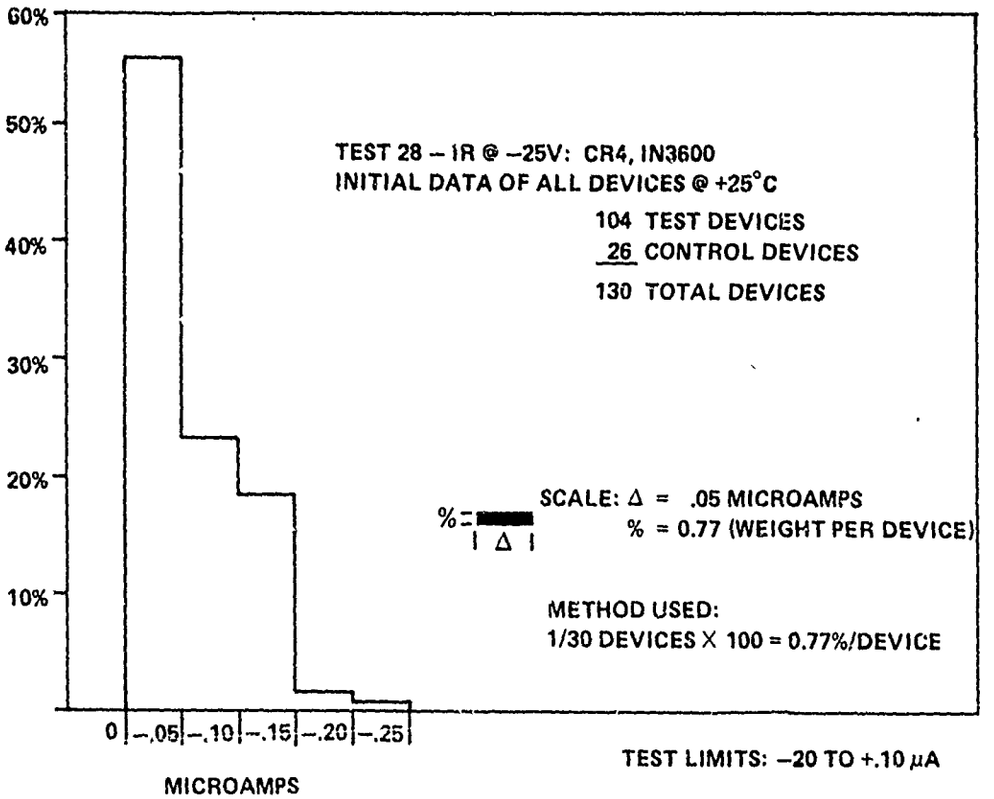


Figure D-7 - Test 28, Initial 25°C Data

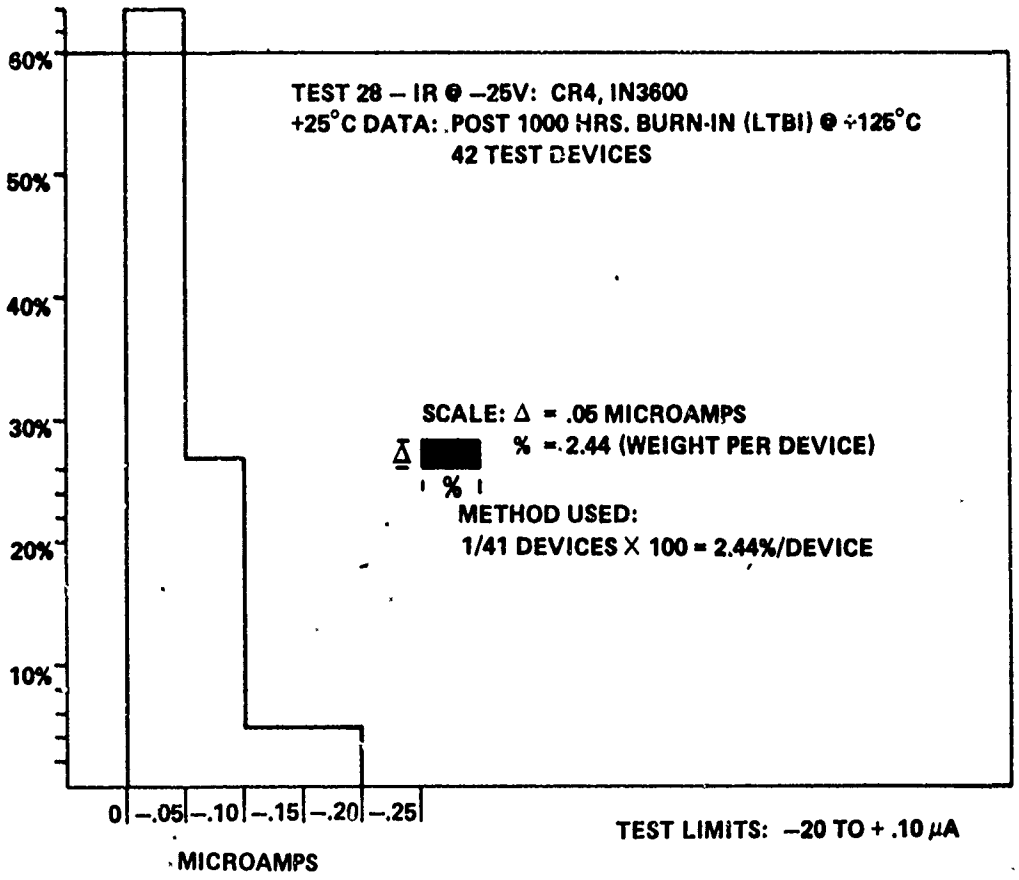


Figure D-8 - Test 28, Post 1000 Hours at 125°C Data (25°C)

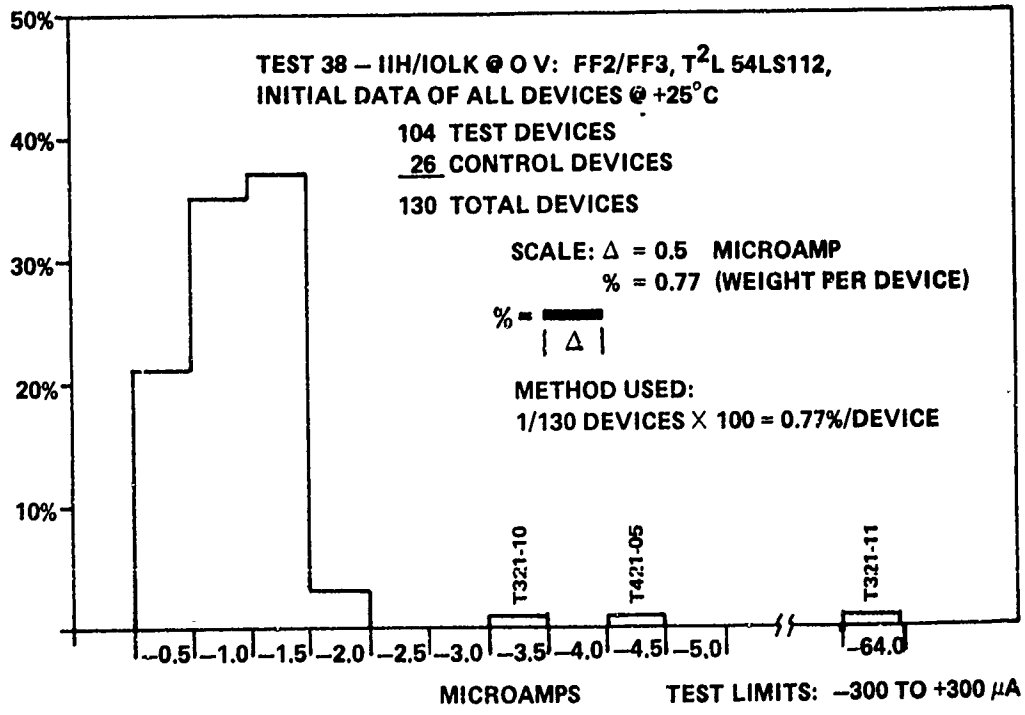


Figure D-9 - Test 38, Initial 25°C Data

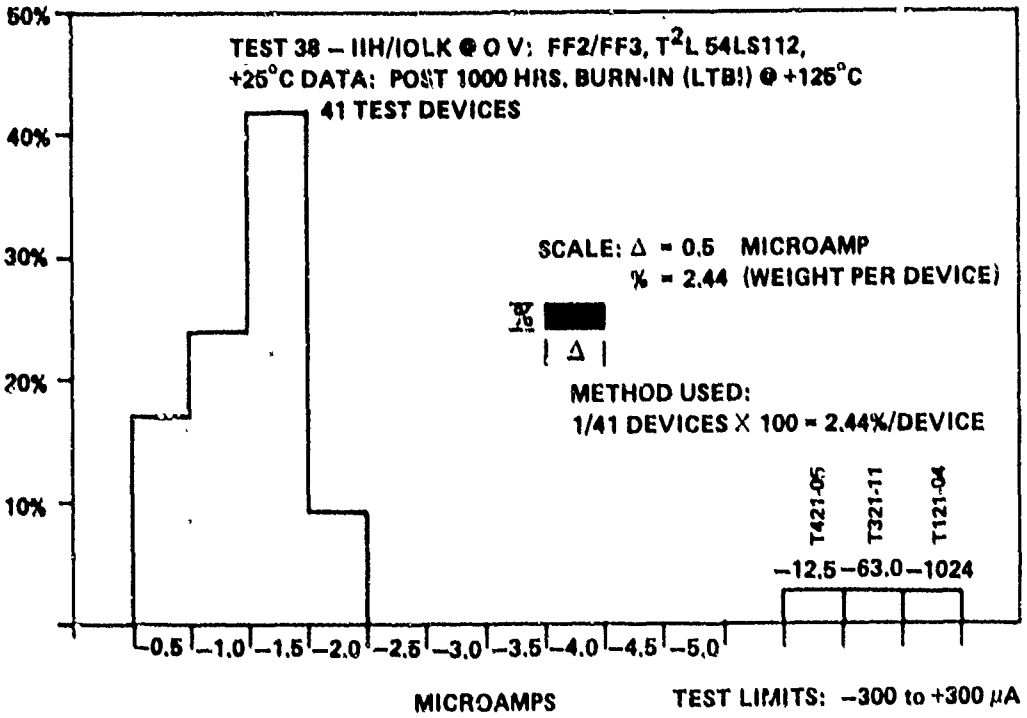


Figure D-10 - Test 38, Post 1000 Hours at 125°C Data (25°C)

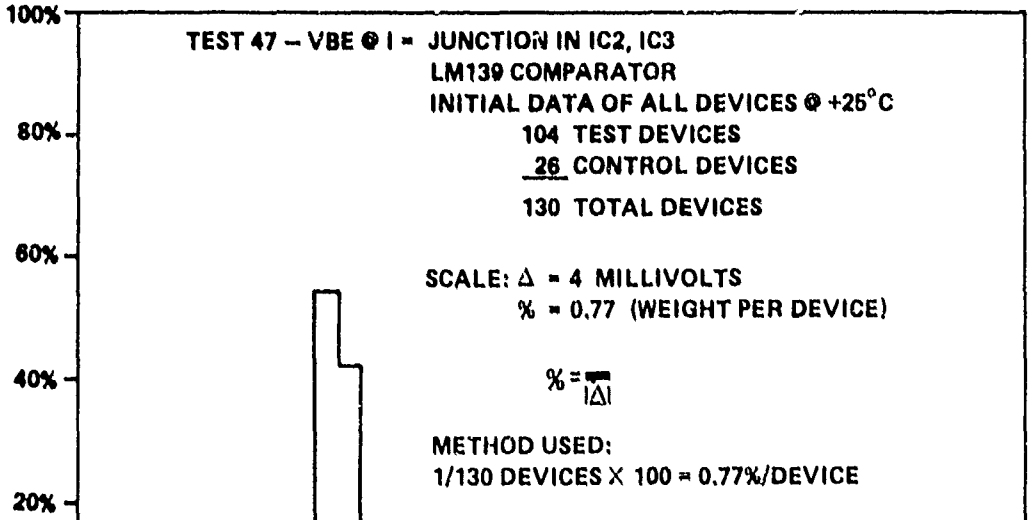


Figure D-11 - Test 47, Initial 25°C Data

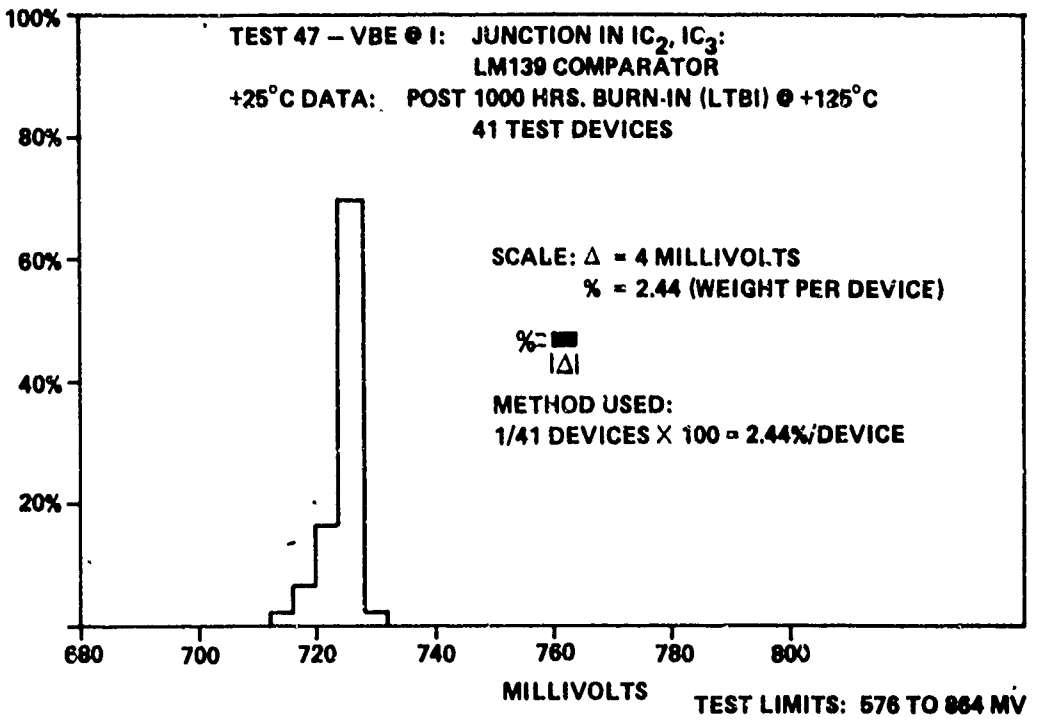


Figure D-12 - Test 47, Post 1000 Hours at 125°C Data (25°C)

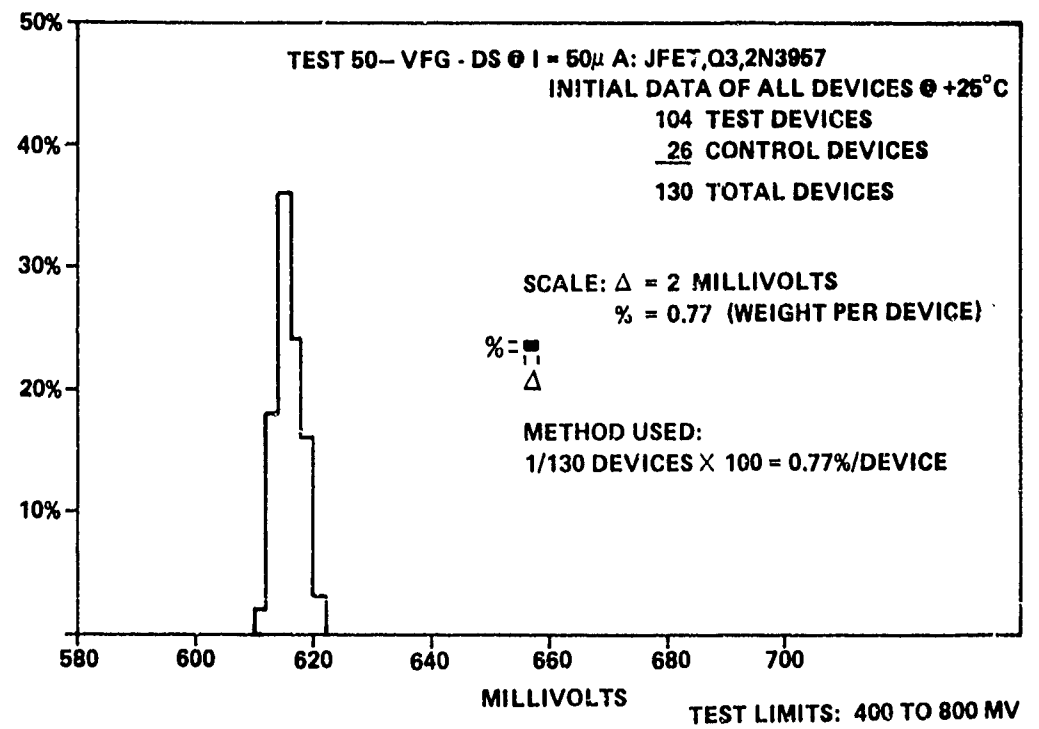


Figure D-13 - Test 50, Initial 25°C Data

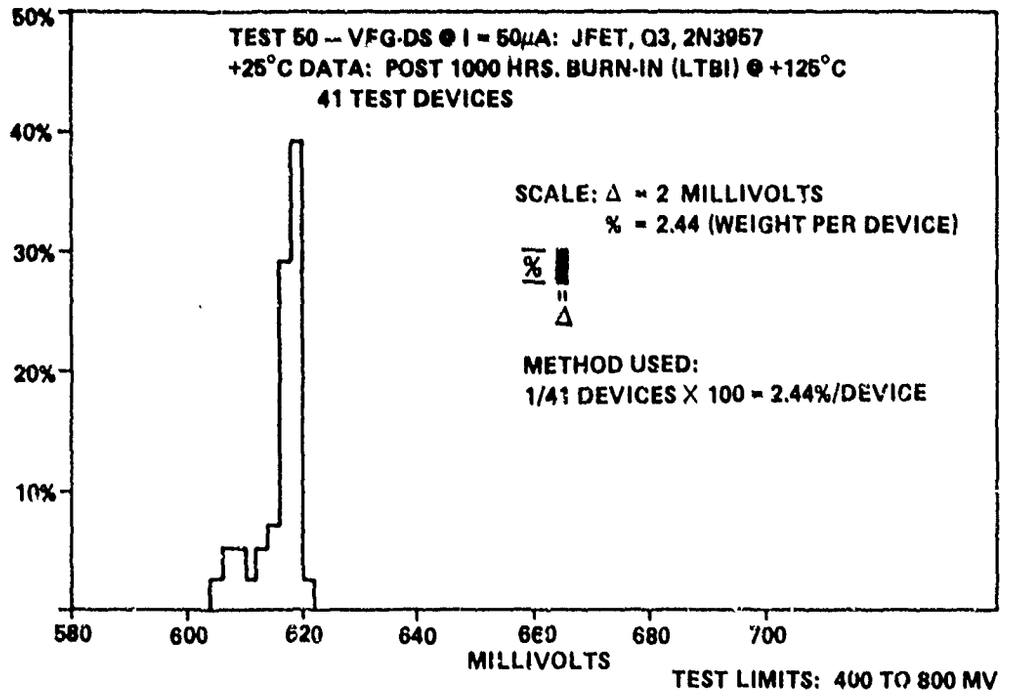


Figure D-14 - Test 50, Post 1000 Hours at 125°C Data (25°C)

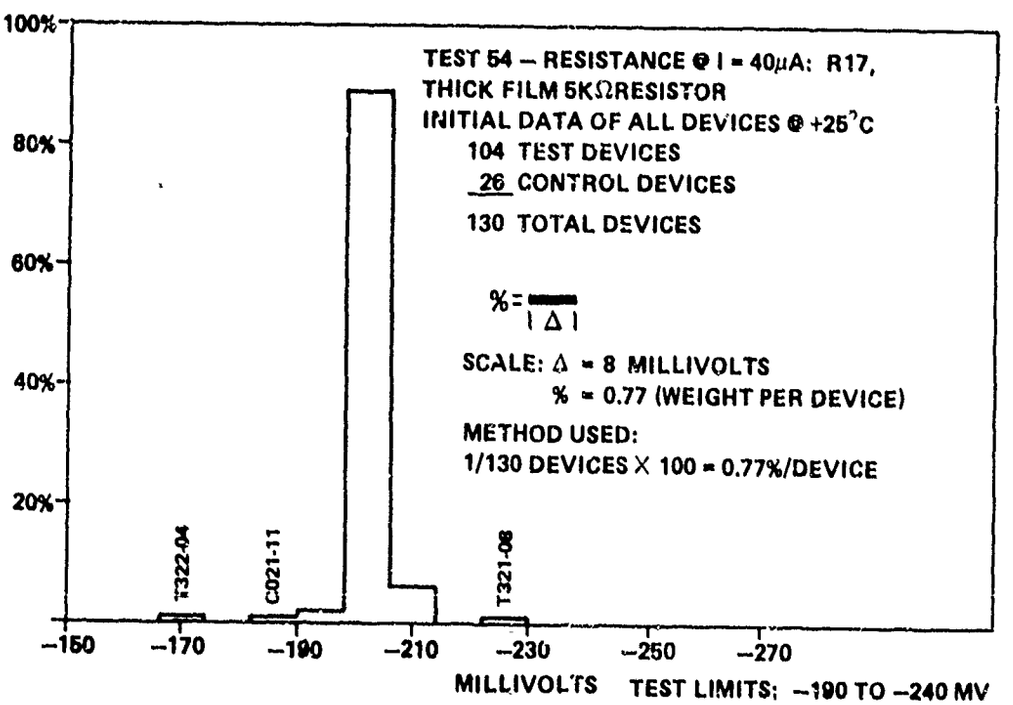


Figure D-15 - Test 54, Initial 25°C Data

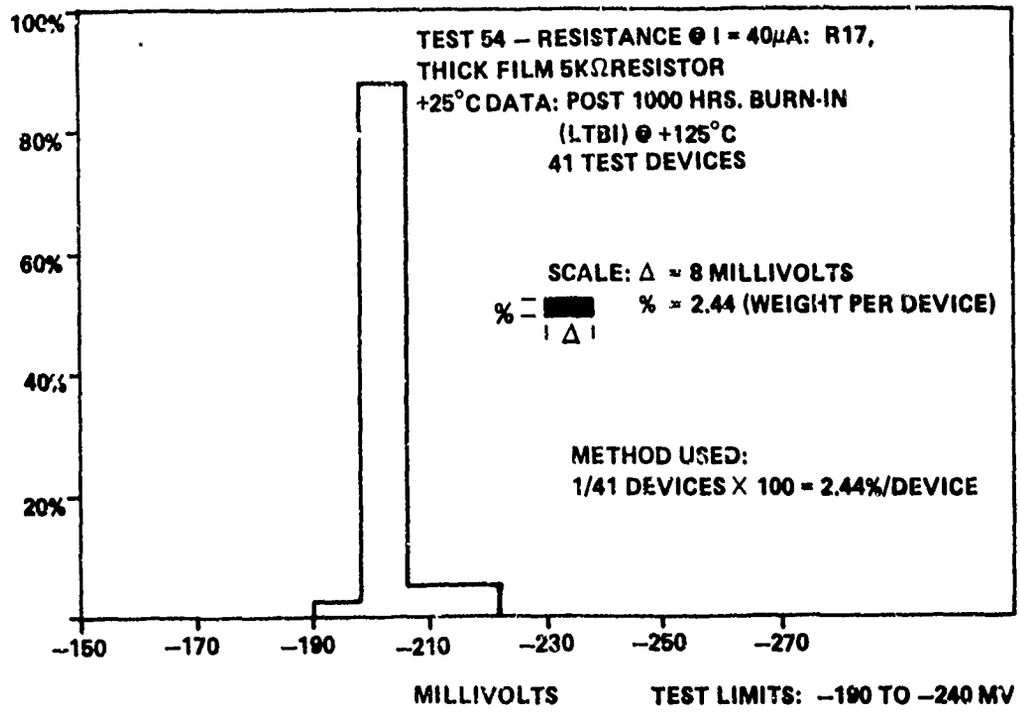


Figure D-16 - Test 54, Post 1000 Hours at 125°C Data (25°C)

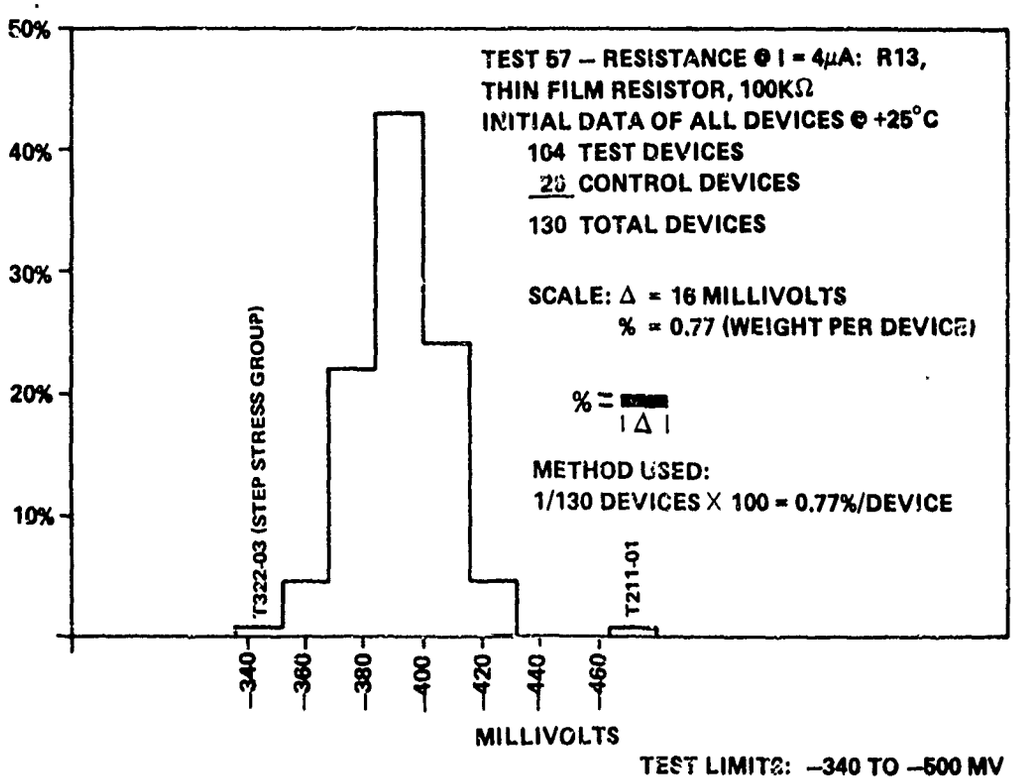


Figure D-17 - Test 57, Initial 25°C Data

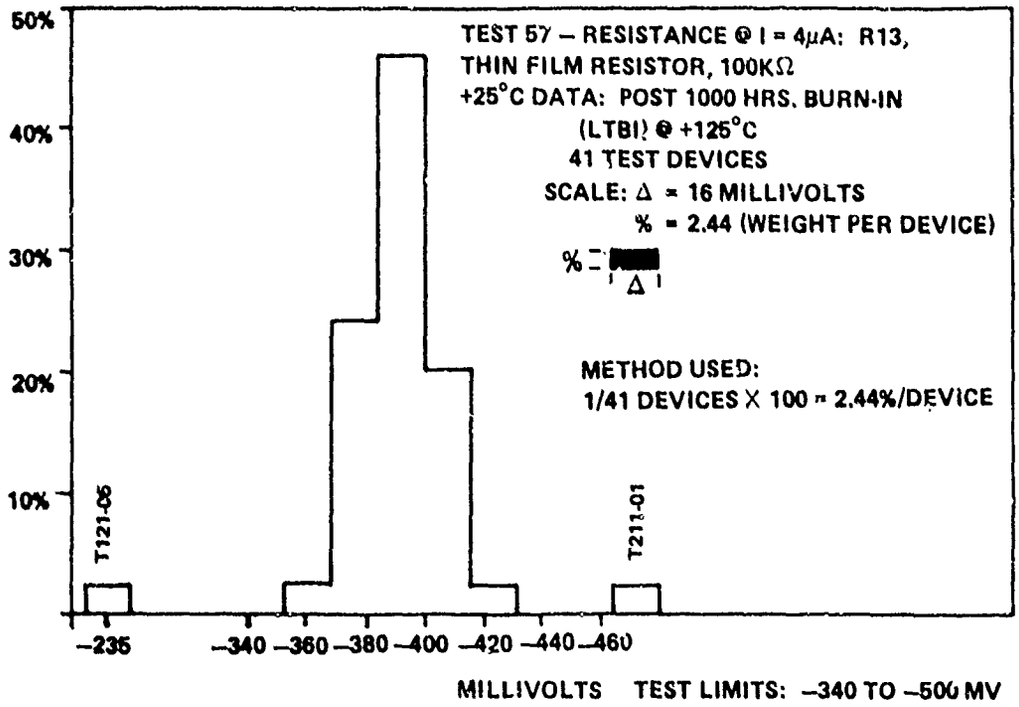


Figure D-18 - Test 57, Post 1000 Hours at 125°C Data (25°C)

APPENDIX E
FAILURE ANALYSES

The failure analysis report included in this Appendix describes failure analyses performed on six hybrid circuit test vehicles. Four of these analyses were performed on devices that were classified as parametric shift failures after 1,000 hours of life testing at 125°C. These included T111-07, T121-05, T421-12 and new control serial number 146. In addition to the parametric failures, analysis was performed on the one device that failure functionally after 500 hours of life testing at 125°C, device T211-13. Also, analysis was performed on control devices that were electrically overstressed and had to be removed from the experiement.

Failure analysis revealed that two chips were overwhelmingly responsible for parametric shift failure. These were the CMOS CD4007 digital IC, and the LSTTL 54LS112 digital IC.

RAYTHEON

PRODUCT ASSURANCE EVALUATION LABORATORY
FAILURE ANALYSIS REPORT

71-0758(4-77)

REPORT NO 783.750

COMPONENT/MATERIAL IDENTIFICATION

NOMENCLATURE	ARMY PART NO	MANUFACTURER	MANUFACTURER'S PART NO.
Hybrid Test Device	31477	Raytheon	31477
REQUISITION	**NEXT HIGHER ASS'Y PN**	**NHA NOMENCLATURE**	**NHA SERIAL NO**
J. DiNitto	–	–	–
DATE CODE/SERIAL NO.	**MAJOR END ITEM/PROGRAM**	**QUANTITY / SCHEM. SYMBOL**	**DATE SUBMITTED**
See Below	Evaluation/RADC	6 / –	3/23/78

FAILURE DESCRIPTION

FAILURE DOCUMENT NO	OPERATING CONDITIONS	FAILURE LOCATION	DATE OF FAILURE
None	Evaluation	P.A. Test	Various
INDICATION OF FAULT	**REMARKS**		**D O NO**

ANALYST'S OBSERVATIONS/COMMENTS:

Six test hybrids packaged as shown in Figure 1 were subjected to failure analysis. Figure 2 is an electrical schematic of the unit, with the IC's labeled. Below is a discussion of the analyses performed:

S/N T111-07 (#138)

After 500 hours of long term life test the voltage at the output of IC4 during V_{OL} testing was noted to have increased to 192mV (Spec. = 1 to 15mV). The unit was electrically operated on the bench with the required supply voltages and the input pins were connected in such a manner as to result in the desired low output at IC4. (see Figure 3). A voltage of 318mV was measured, verifying the failure. The unit was physically opened by cutting through the device lid. An internal visual inspection of the unit and in particular of IC4 and I2 failed to reveal any visual abnormality to account for the malfunction. The bond wire connecting the output of IC4 and the input of I2 was lifted, isolating the two gates. Retesting the unit revealed the output characteristics of IC4 to be unchanged, verifying the failure to be IC4.

CAUSE

See summary of failure analysis. Failures isolated to specific chips.

- ☐ VENDOR PROCESS
- ☐ TEST ERROR
- ☐ VENDOR PROCESS HUMAN FACTORS
- ☐ OTHER (SPECIFY)
- ☐ VENDOR DESIGN

CAUSE IDENTITY QUALIFICATION

- ☐ UNKNOWN
- ☒ SUSPECTED
- ☐ GOOD CASE
- ☐ CONFIRMED

RECOMMENDATION

None.

RECOMMENDED ACTION

INVESTIGATE

- ☐ VENDOR
- ☐ STUDY ADD'L EVIDENCE
- ☐ CIRCUIT
- ☐ MASK CONTROL
- ☐ OTHER (SPECIFY)
- ☐ PROCESS

/db	ANALYST (TYPE)	x4301 CS1-62	SIGNATURE	DATE
	W. Weise		W. Weise	3/30/78

ANALYSTS OBSERVATIONS/COMMENTS

S/N T121-05 (No. 101)

This unit was found to fail V_{OH} at the output of IC4 after 500 hours of long term life test. A value of 0.26 volts was measured (Spec. = 4.9 to 5.1 volts). Electrical testing of the unit on the bench revealed that by controlling the logic levels into IC3, an output high was not possible from IC4. An analysis of the logic levels at the output of IC3 revealed that the logic high value obtained was only 1.5 volts, rather than the expected value of 5.0 volts (see Figure 4). The unit was opened by grinding through the device lid. A visual examination of the surfaces of IC3 and I2 revealed no visual abnormalities to account for the device failure. The bond wire to the input of I2 was disconnected and the unit was retested (see Figure 5). The output voltage was observed to go to the expected 5.0 volts.

T421-12 (No. 125)

After 1000 hours of long term life test this unit was found to fail electrical test. The short-circuit current at the non-inverting output of FF4 was measured to be 2.05 mA (Spec. = 15 to 100 mA) and the output low FF1 was measured to be 1.02 volts (Spec. = 0.05 to 0.4 volts). Electrical testing of the unit revealed the outputs of FF4 to be latched. No other abnormalities were noted. The unit was physically opened and the flip-flops visually examined. No visual cause of failure was observed. The latching of the FF4 was the result of the failure of FF3 or FF4 (both on same chip). No evidence of failure was observed at FF1.

Control Unit (No. 146)

This unit failed after 240 hours of Sealed Lid Burn-In (SLBI). The primary cause of failure was the observance of incorrect logic values to the output of IC4. Output Low = 39 mV (Spec. = 1 to 15 mV) and Output Hi = 0.155 volts (Spec. = 4.9 to 5.1 volts). Electrical testing of the unit revealed electrical characteristics at the output of IC4 similar to those observed for T121-05. The unit was physically opened and visually examined. No visual evidence to account for the failure. The bond wire going from IC4 to I2 was open-circuited and the unit retested. The characteristics observed were within specification, indicating that the gate oxide to the input transistors of I2 was degraded.

S/N T211-13 (No. 139)

After 500 hours of long term life test, the voltage at the output of IC4 was noted to have increased to 254.5 mV (Spec. = 1 to 15 mV). The unit was electrically tested on the bench with the logic configured so that a low was observed at the output of IC4. A value of 200 mV was observed (see Figure 6). Unit was opened and the bond wire connecting IC4 and I2 was disconnected, isolating the two gates. The output of IC4 was retested and found to be unchanged. A visual inspection of the IC4 chip revealed no apparent defect to account for the failure.

S/N C021-10 (No. 7)

This unit was representative of a group of control devices found to be failed after 240 hours of Sealed Lid Burn-In. Pin 2 (+12 V) was reported to be open-circuited. Bench testing verified this failure. The unit was opened and a visual examination revealed the bond wires from pin 2 had been vaporized and the associated NPN transistor was no longer attached. (See Figure 7). The unit was apparently overstressed at pin 2.

Summary of Failure Analysis

S/N	No.	Failure Location
T111-07	138	Output Section of IC4
T121-05	101	Degradation of Input Gate Oxide I2
T421-12	125	FF3/4 I.C. Failure Verified
Control	146	Degradation of Input Gate Oxide I2
T211-13	139	Degradation of IC4
C021-10	7	Overstressed pin 2

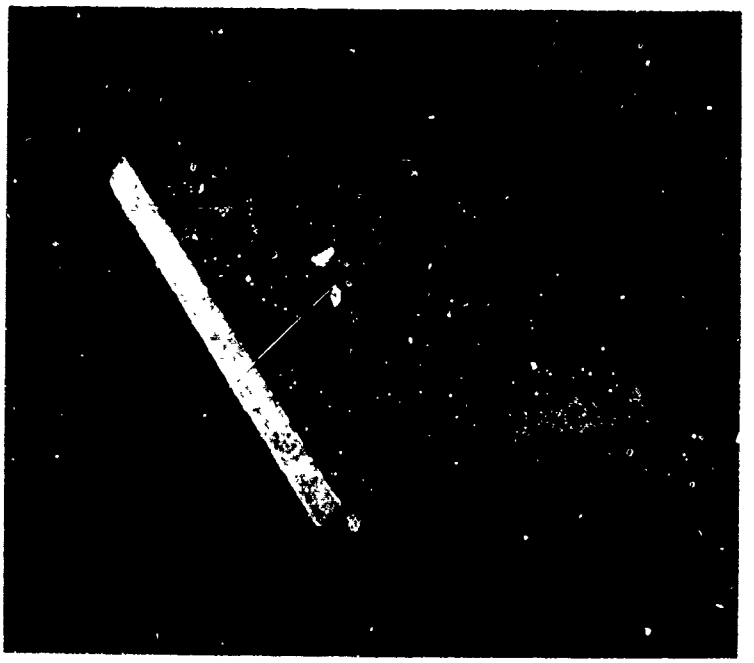


Figure E-1 - One of the Devices Received (2X Magnification)

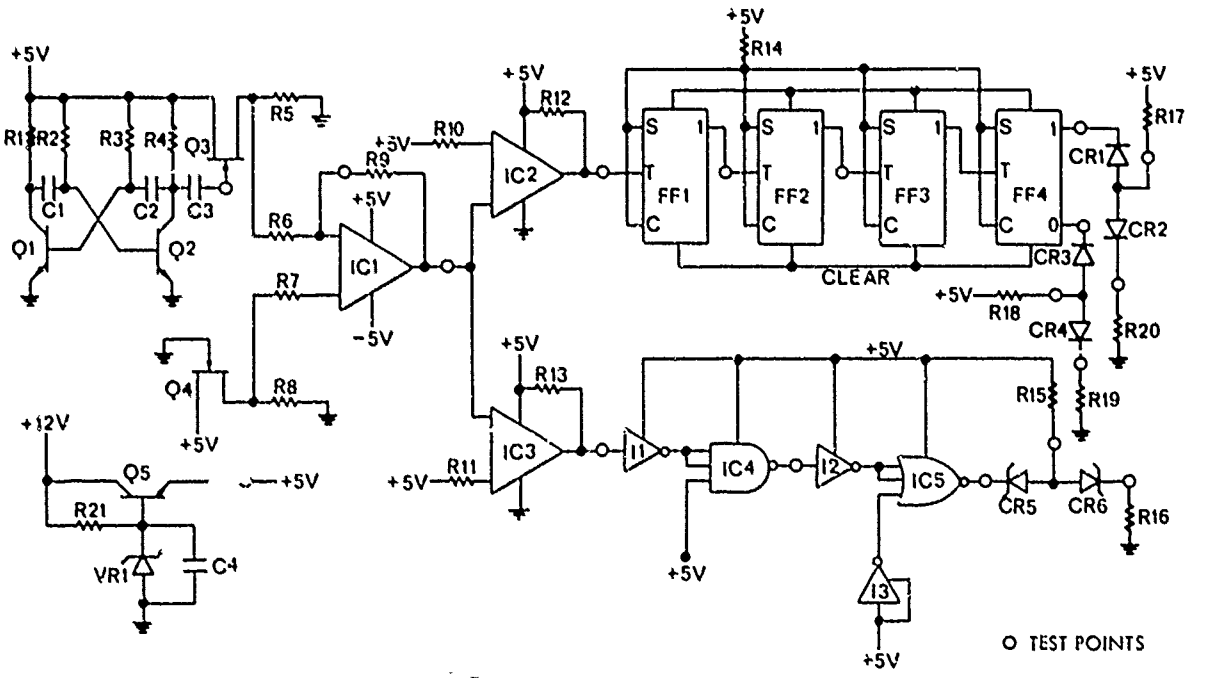


Figure E-2 - Electrical Schematic of Device With Integrated Circuits Labelled

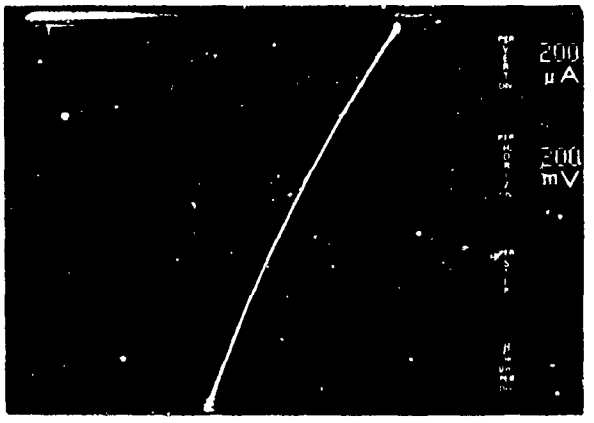


Figure E-3 - T111-07, Current-Voltage Characteristics Observed at Output of IC4 (IC4 is in a Low State) Center of Gradicule = 0

Figure E-4 - T121-05, Current-Voltage Characteristics, Observed at Output of IC3 With Multivibrator Running (Center of Gradicule = 0)

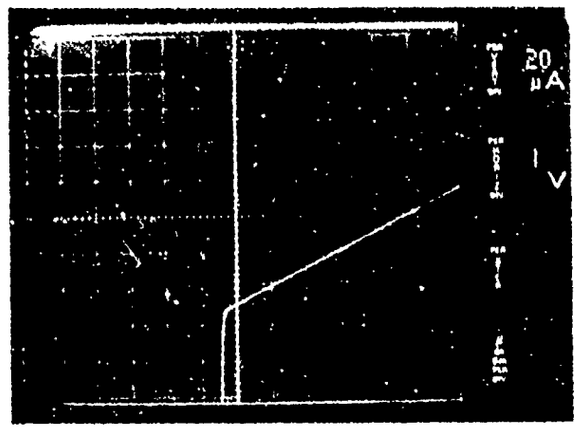


Figure E-5 - T121-05, Current-Voltage Characteristics Observed At Output of IC3 With Multivibrator Running (Note: Input To I1 Has Been Disconnected) Center of Gradicule = 0

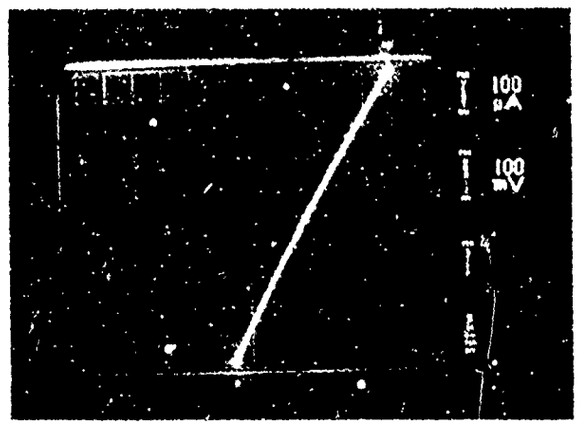


Figure E-6 - T211-13, Current-Voltage Characteristics Observed At Output of IC4 (IC4 Is In Low State) Center of Gradicule = 0

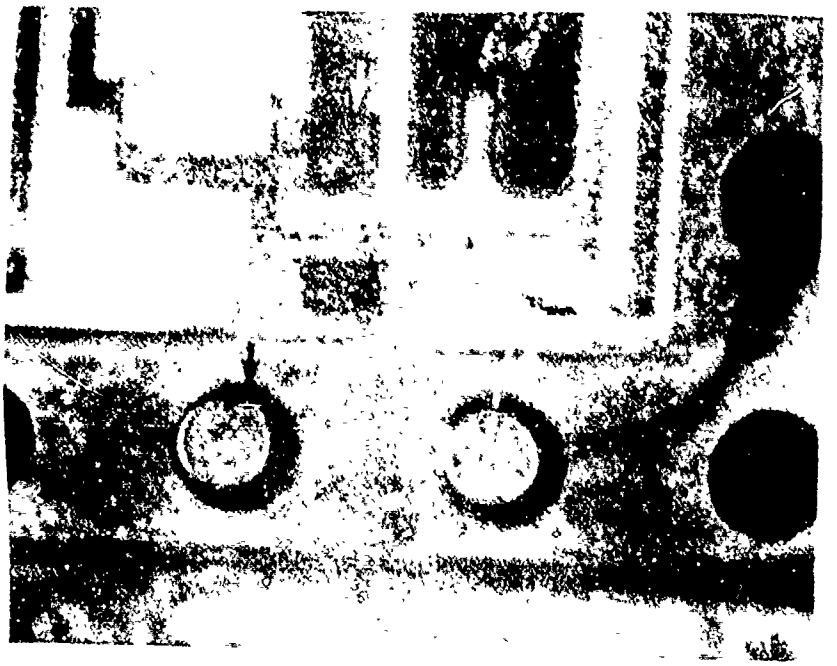


Figure E-7 - C021-10, Photo of Open-Circuited Bond Wire At Pin 2 (Black Arrow) and Missing Transistor (White Arrow) 15X Magnification

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